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A COOPERATIVE TERMINAL INFORMATION TRANSFER SYSTEM

TECHNICAL REPORT AFAL-TR-74-322

DECEMBER 1974

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AIR FORCE SYSTEMS COMMAND
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This technical report has been reviewed and is approved for publication.

Blinn W. Russell

BLINN W. RUSSELL
Project Engineer

FOR THE COMMANDER

Charles C. Gauder

CHARLES C. GAUDER
Acting Chief
Information Management Branch
System Avionics Division

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The report proposes a digital synchronous internal information transfer system for relatively unsophisticated USAF aircraft. A detailed description of the design, and its application to a specific example (a postulated A-10 avionics suite), are provided.

An inexpensive clock reference coordinates bit timing at the terminals, permitting the elimination of a central bus controller and supervisory

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(overhead) words on the bus. The transmission rata is much lowar than that usually encountered, made possible by (1) aliminating the overhead words, (2) doing away with (inefficient) word packing on the line, and (3) achiaving a high bus loading (utilization) factor by a bit-time slot allocation scheme unique for tha application.

The lower oparating fraquency should alleviata bus-to-tarminal impedance matching and line coupling problems.

The proposed use of replacaabla (plug-in) memories for storaga of tha system operating parameters probably will permit a high degraa of circuit standardization (interchangeability) within the tarminals.

It is concludad that the system should ba simplar, more dependable and less expensive than alternate multiplex methods for tha stated application.

An in-house experimental program to verify tha dasign is recommended

FOREWORD

Appreciation is expressed to Mrs. Sybil Hooper, AFAL/AAM, for her diligent work in the typing of the manuscript and the final copy of this report.

SUMMARY

The purpose of this theoretical investigation was to devise an internal aircraft information transfer system (ITS) suitable for smaller, less sophisticated USAF aircraft. The RPV and A-10 are mentioned as possible applications. The primary objective was to provide simplicity of design; thereby minimizing cost of ownership while achieving highly reliable and error free operation. Cost of ownership was taken to include original investment plus maintenance costs including avionics modification and retrofit programs. The work was accomplished as an in-house effort by Mr. Blinn Russell of the System Avionics Division, AFAL/AAM.

The ITS essentially consists of several terminals strategically located about the aircraft so as to be adjacent to concentration of avionic equipments (subsystems, SS), and an interconnecting shielded twisted wire pair data bus. The purpose is to transfer serial digital signals, i.e., binary digits or "bits", between large numbers of user pairs (sources and sinks) located within the SS's. The bits are transported over the bus on a time shared basis without mutual interference. The ITS as described in the report excluded the signal converters in the terminals, usually referred to as Subsystem Interface Units, SSIU's, which transform the myriad of SS signal formats to serial digital. Also, the details of the transmitter and receiver "front ends" involving baseband modulation and detection and bus to terminal coupling/decoupling required for interfacing with the transmission line were not of direct concern in the investigation. Attention was concentrated on the traffic

management area. This included a systematic apportionment of the bits to time slots on the line, and examination of the timing and control requirements of the terminals.

Each binary digit has a specific time slot on the bus. It is identified as to its SS source and sink by its relative position in time on the line, and its predetermined locations in the buffer memories of a transmitting terminal and of a receiving terminal. The report focuses on Timing and Control (T & C) Units, one per terminal, whose functions are to (1) transfer the bits onto and off of the bus at the proper instants in time and (2) route them into and out of the proper addresses in the buffer memories.

An inexpensive clock reference coordinates the timing of the T & C Units. This design approach permitted the elimination of the central bus controller usually specified for systems of this type, and all supervisory (overhead) words on the bus. The transmission rate is much lower than that normally encountered; made possible by (1) eliminating the overhead, traffic control words, (2) doing away with the usual standard information word format and its attendant poor packing factor for smaller signal sets, and (3) achieving a high bus loading (utilization) factor by a bit-time slot allocation scheme believed to be new for this application.

The matter of clock "skew", namely, that of maintaining phase coherence for reliable detection over varying lengths of the bus, was examined. It was concluded that skew would not be a problem for data rates as high as 275 KHz and cable lengths up to 50 feet.

Built in Test (BIT), status reporting and error detecting considerations were beyond the scope of the report. With those exclusions, the clock (data) rate on the bus would be the same as the information transfer rate of the system.

Achievement of a lower data rate and hence a narrower bandwidth on the bus was a principal design objective. Its purpose was to provide more reliable operation by alleviating wide band bus-to-terminal impedance matching problems which are the cause of waveform distortions, pulse jitter and other impediments to error free operation.

Important cost saving items are (1) a type of standardization which minimizes the number of subassemblies which must be procured and (2) simplified ITS adjustment procedures when there is modification or retrofitting of the avionics suite. A design feature is the use of replaceable (plug-in) read only memories for storage of the system operating parameters. This permits the Timing and Control Units at all the terminals to be permanently wired (also of the plug-in module type) and identical. Reserve memory capacity is provided sufficiently large to accommodate any foreseeable increase in user load for the vehicle. Retrofit requires only computation of a new signal flow chart, the burn-in of new plug-in memory cards, and their insertion in the terminals.

The "paper" design of the report is detailed to the level of functional block diagrams. The seven major components of T & C which effect the memory to bus and bus to memory transfers are diagrammed, and their step-by-step operations are fully described in the text. The technical approach was applied to a postulated avionics complement for the close air support Night AX, now the A-10, using the signal flow

tables for that aircraft supplied by SCI Systems, Inc. on Contract F33615-71-C-1918, "Information Transfer Techniques for the Night AX."

SCI's raw signal flow data were reworked to derive the basic operating parameters, and the results were tabulated. The method of allocating bits to time slots on the bus such that all pre-specified sampling rates are maintained and the line is essentially fully loaded is described.

The design is intended to include sampling rates up to 400 samples/sec, S/S (400 Hz); and the SCI model, essentially, specified rates of 400, 200, 100, 40, 20, 10 5 and 1 S/S. The example was scaled down to make it amenable to hand computations, by eliminating the 400, 200 and 100 values which, however, only reduced the size of the original SCI signal set by less than 2%. For this example, a bus utilization factor of 98.4% was achieved.

This same AX (A-10) example has been applied to three diverse multiplex methods, (1) command/response mode, SCI, Contract F33615-71-C-1918, (2) the RUSMUX concept by the author, AFAL-TR-73-133, "A New Data Distribution System for Aircraft", and (3) the system of this report. The stage is now set for a quantitative, experimental comparison of the three methods in the laboratory. A combined breadboard and computer simulation program to accomplish this is recommended.

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I. INTRODUCTION

PURPOSE OF THE REPORT

This report results from a conviction that multiplex systems alternate to Command/Response should be investigated in more detail than has been done heretofore. Schemes the writer has in mind may offer advantages over that of MIL-STD-1553 (USAF), (1), for some applications. One of the proposed systems, a synchronous cooperative terminal arrangement, is described and discussed in the report.

The basic ideas set forth are believed to be both practicable and philosophically sound. Some work remains to be done on the method of implementation. Hopefully, the approach can be proved out in the laboratory, as suggested under RECOMMENDATIONS.

DESCRIPTIVE MATERIAL

The report describes a synchronous digital information transfer system (ITS) for smaller and possibly medium sized USAF aircraft of the less sophisticated types. No central bus controller is required. The avionic signal sampling rates are those with bandwidths up to 400 Hz. Such signals are generally agreed upon to be the prime candidates for Time Division (TD) multiplexing (muxing) on a twisted wire pair, (1), para. 10.3.

Excluding Built in Test (BIT) status reporting, error detection, and other similar considerations which must be dealt with at

(1) Military Standard "Aircraft Internal Time Division Multiplex Data Bus", MIL-STD-1553 (USAF), 30 Aug 73.

some later date, the bit rate on the time shared data bus is the same as the true terminal-to-terminal information (info) transfer rate. That is, there is no supervisory or traffic control overhead on the bus. This contrasts with such systems as Command/Response, where the overhead may range from 50% on a large aircraft to as high as 75% on smaller ones.

This is not a polling or "contention" method of gaining access to the data bus. That approach no longer is seriously considered for internal aircraft multiplex systems.

A centrally located clock in the aircraft, operating at the bit rate, tightly controls the timing of the entire system. The stability requirements on the clock are not at all severe, and it should be inexpensive. Also, it should be a simple matter to provide a standby clock, available if the primary fails.

The clock pulses, either on a separate wire in the bus or possibly on the same twisted pair as the data, are picked off at the terminals. There they synchronize (sync) Timing and Control (T & C) Units. T & C's functions are to (1) provide for the transfer of the proper bits onto the bus at the proper times, and (2) correctly route incoming bits into their right locations in buffer memories. In a one second main period, all ultimate signal sources in the avionic equipments in the aircraft suitable for muxing are sampled and the readings transferred at the rates specified in signal flow charts. This is a basic requirement of the ITS. Each bit has its own allocated time slot in the one second interval.

The signal transportation requirements are met while also maintaining the time shared data bus essentially fully loaded in the process. The way this is done is a salient point in the design.

Emphasis in the report is on the Timing and Control processes and circuits.

A unique waveform, occurring once per second in the bit clock sequence, serves as a sync pulse to time the starts of the repetitive main period at all terminals.

To provide interchangeability, flexibility and circuit standardization with resulting lower ownership costs, the values of the system operating parameters which correspond to the particular avionics complement in the aircraft, are stored on replaceable (plug-in) memory modules.

CENTRAL VERSUS DISTRIBUTED CONTROL

Multiplex systems are sometimes classified as either being centrally controlled, or having distributed control. The proposed ITS lies between these two extremes. There is an important central control aspect in that a central bit clock is required. On the other hand, the preponderance of the traffic management is done at the terminals on a collaborative basis. Hence the name "cooperative terminal" system.

LONGER TERM OBJECTIVE

A philosophical approach to the design of a new class of federated, or distributed control mux systems, RUSMUX, was presented last year in (2). That report suggested the simultaneous encoding of

(2) "A New Data Distribution System for Aircraft", AFAL-TR-73-133, Blinn W. Russell, July 1973

avionic signals in the frequency, space and time domains. This would be done in such a manner that the signals are conveyed over a common multiconductor bus in essentially independent subsets, without mutual interference.

As a part of (2), the author applied the RUSMUX concept specifically to the A-X, now the A-10, using signal lists provided by SCI Systems, Inc., in (3). Also in (3) SCI used those lists in a preliminary design of a Command/Response multiplex system for the A-10.

Thus, with the completion of the paper design of the cooperative terminal ITS described in this report, three fundamentally different design approaches (Figure 1) have been applied to the same physical example, namely, an A-10 Avionics suite. To the best of the author's knowledge, this is the first time that data of such a nature, to such a high degree of specificity, has become available. Hopefully follow-on comparison tests of the three techniques using the MUX Simulator can be conducted within the next several months.

In a sense, the cooperative terminal approach, the central block of Figure 1, is a bridge between the other two development and design routes. In addition to containing elements of both, it appears to represent about the highest degree of symmetry achievable, with regard to processing the data over the bus. The information flows at a uniform rate. It may, as time passes, come to serve as a convenient benchmark against which other systems can be compared.

(3) "The Application of Information Transfer Techniques for Solving the Internal Communication Requirements of a Night AX Aircraft", AFAL-TR-72-289, Volumes I and II, Contract F33615-71-C-1918, SCI Systems, Inc., April 1973.

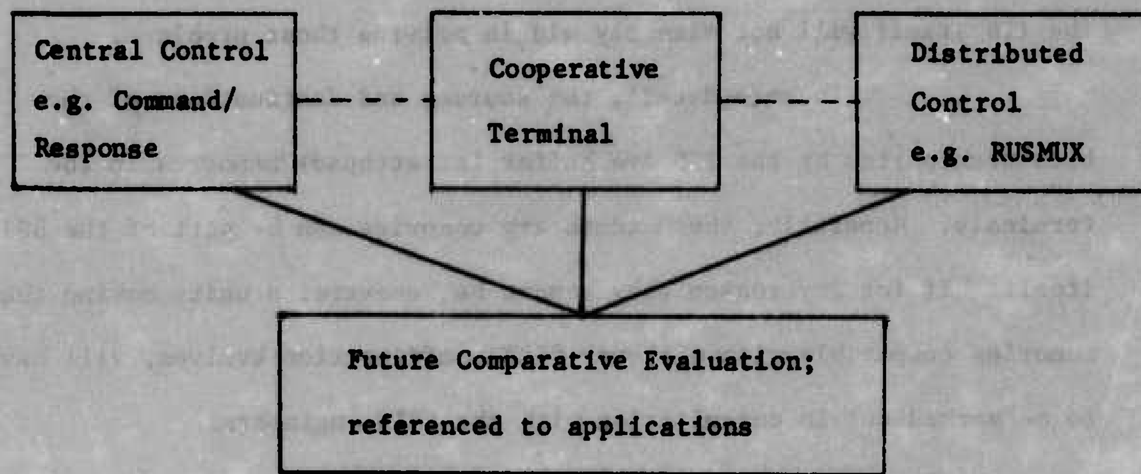

FIGURE 1. Alternative Multiplex Techniques

TREATMENT OF AN AIRBORNE COMPUTER

Although the postulated A-10 configuration upon which the example is based contained no special or general purpose computer, such a unit might well be present in semi-sophisticated aircraft to which the design approach applies. Wherever that is the case, the computer is treated exactly like any other avionic equipment insofar as the ITS is concerned, and no particular problems are anticipated. That is, it is another subset of data sources and sinks, relative to the bus line.

INPUTS AND OUTPUTS OF THE ITS

It is recognized that a large percentage of the technical problems of the DAIS lies in the design of the Subsystem Interface Unit, SSIU, (1), para. 3.3. The area of concern of this report is elements of the (per Mil Std terminology) Multiplex Terminal Unit, MTU. Assumed inputs and outputs are the outputs and inputs (toward the bus)

of the SSIU; and obviously even a "quantum jump" in simplification of the ITS itself will not directly aid in solving those problems.

In more detail, the sources and destinations of the bits transported by the ITS are buffer (scratchpad) memories in the terminals. Hopefully, these temporary memories can be part of the SSIU itself. If for any reason they cannot be, conversion units making the memories compatible with whatever SSIU configuration evolves, will have to be worked out in consultation with the SSIU engineers.

A SALIENT DESIGN FEATURE

Five computer-like operations are performed in each terminal in connection with traffic management. All of them involve the processing of sets of numbers, referred to as operands. They include the epochs (points in time) at which the terminals individually transmit and receive, and the memory addresses needed to route information bits into and out of buffer memory. The sets of operands are peculiar to the avionic complement of the aircraft. In addition, for four of the five operations a different set of operands is required at each terminal. For the fifth wired-in instruction, the operand set is the same at all terminals. This is spelled out in Section II.

To provide flexibility, the operand values are stored within the terminals on plug-in read only memory (ROM) cards which can be changed by AF Flight Line or Depot Maintenance personnel. This would be done, for example, if modifications were made in the composition or arrangement of the avionics suite in a retrofit program. No rewiring in the terminals would be required.

With the above feature, the computer instructions and the

circuits by which they are executed, can be permanently wired into the terminals.

The "black boxes" which accomplish the circuit functions most likely will be solid state integrated circuits. These modules also could be the plug-in type for ease of maintenance.

Thus, the solid state Timing and Control (T & C) circuits in all terminals probably would be identical, a form of standardization which should result in appreciable cost savings. Conceivably, if the system is widely adopted, the same T & C Units could serve for a class of aircraft which are approximately the same type.

CLOCK SKEW

A concern sometimes voiced with regard to a sync'd system, is the matter of clock skew. The propagation time on a wire pair is finite, being approximately one nanosec per foot, (4), page 171. Hence clock pulses emanating from one point in the system arrive at the terminals with varying delays, depending on their distances from the clock. As a result there can be a slight overlap of adjoining pulses received by one terminal from different transmitting terminals. This is a source of a small amount of intersymbol interference. A detailed noise analysis, not reproduced here, has indicated that relatively low bit error rates (10^{-9} or less) would obtain if the bus length does not exceed 50' and the data rate 275 KHz. 50' is the cable length required for the A-10 aircraft. 275 KHz is a bit rate which is more than 15 times that of the example in the report.

(4) Digital Systems: Hardware Organization and Design, F. Hill and G. Peterson, John Wiley and Sons, 1973.

POTENTIAL SYSTEM ADVANTAGES

It is felt that the data rate on a wire bus should not be as high as the 1 MHz specified in the Mil Std whenever that high a rate is not necessitated by the size of the signal set. Several important technical difficulties can be alleviated by operating at a lower frequency. Some of these are described and discussed in Appendix A.

It is further felt that the rate can be several times lower (than 1 MHz) in small and medium size aircraft using the cooperative terminal mux design. This is for the following reasons:

(1) There are no supervisory words on the bus.

(2) There is no word structure on the bus. Transmission is bit-by-bit. Hence there is no inefficient word packing as is often encountered when the signal set is of moderate or small size.

(3) The signal set itself obviously is smaller in smaller, lower performance aircraft.

Bit Allocations on the Bus. The cooperative terminal approach lends itself to a pattern of bit assignments to the line such that the line essentially is fully loaded or "working" all of the time. A load factor, often called a Bus Utilization Factor (U.F.) is defined as the percentage of time the bus is loaded. A U.F. of 98.4% was achieved for the example. A high U.F. implies minimum bandwidth for a given data rate, with several resulting technical advantages as detailed in Appendix A.

Less Circuitry, Possibly Greater Reliability. Bits are identified by their relative positions in time. This would seem to be about as elementary a design as one could come up with. Eliminating

the Bus Controller also does away with considerable control word coding and decoding hardware at every terminal. There being no information word structure eliminates further hardware. Lowering the bit rate drastically on the line while filling the line with info bits can greatly increase the energy per bit. Theoretically this would reduce the probability of error due to noise, for a given signal level. As a tentative judgment, these and other factors mentioned above could materially reduce the cost and increase the reliability compared to Command/Response.

II. TIMING ON THE BUS (Applied to the A-10 Model)

NETWORK DESCRIPTION

Six terminals, strategically positioned about the aircraft, share the common data bus. Avionic equipments, often called Line Replaceable Units (LRU's) or Subsystems, connect to the terminals in sets, according to their physical locations. Within the LRU's are a large number of signal sources and sinks. The ITS, along with Subsystem Interface Units (SSIU's), provides the means for each signal to proceed from its source, through a terminal, over the bus, through another terminal and into the proper sink, without interference relative to other signals.

Each terminal has a transmitter and a receiver section (defined with respect to the bus). The function of its SSIU is to match the diverse avionics subsystem inputs and outputs to the ITS, including conversion to and from binary when necessary. The basic avionic signals are a mixture of discrete, analog and digital numeric forms. In some cases, although not in the example, synchro voltages are multiplexed.

The digits on the bus each convey one bit of information. Physically they are short bursts of electromagnetic (EM) energy; having

one waveshape for a binary 1 and another for a binary 0.

SIGNAL LISTS

Signal lists, each applicable to a particular type of aircraft, and containing pertinent avionic signal characteristics, are available from various sources. At the present stage of the "game" they usually require considerable re-work and reorganization to fit a specific application. The problem faced by the author in that regard was no exception. Data tabulated by SCI in (3) was the starting point, and the details of the recompilations are given in Appendix B.

SAMPLING RATES

A key column heading on the signal lists is sampling rate, and it is paramount to our plan. For this reason that item is dwelt on in some detail in the paragraphs which follow.

The status or value of some parameter is observed periodically at every source, some number of times per second. The results of the readings are transmitted over the bus at, or close to, the observation rate, called the sampling rate. This is abbreviated in the report as S/S for samples per second. Each source has its own S/S, and there is a finite number of S/S's, of the order of 5 to 10, in a signal list.

Bits are identified as to their sources and sinks solely by their relative positions in time on the bus. Hence they must be ordered on to and off the line in proper sequence to accomplish that function. But in addition, they must be impressed onto the bus in such a pattern that the correct S/S's are maintained. And lastly, a goal is to maintain the line essentially fully loaded in the process. How all this may be achieved, at a very high bus Utilization Factor, U.F., is

explained in the following paragraphs.

MAIN PERIOD, AND S/S's OF THE EXAMPLE

The primary period is one second because the signal data is presented in samples/sec (S/S). The lowest sampling rate is one S/S, hence every source-sink pair is "united" at least once by a data exchange, during the period.

The S/S's must bear an integral multiple relationship for the time slot allocation which follows to be applied. SCI's data, with a couple of minor exceptions were in that form.

The contractor used 400, 200, 100, 40, 20, 10, 5 and 1 S/S. The 400, 200, and 100 values were dropped to scale down the example.

Actually, this only reduced the total signal set from the version of the RUSMUX report (2) from 586 to 576 signals, a reduction of 1.6%. [(2), by eliminating two 32 bits/sec dig/num.'s @ 350 S/S from SCI's original list, had reduced the total bit rate from 47,023 bps to 24,623 bps.]

SLOT ALLOCATIONS

The organization of bits on the bus is determined primarily by the sampling rates, S/S. The numbers of signals and bits at each

Sampling Rate	40's	20's	10's	5's	1's	Totals
Nr. of Signals	3	175	41	234	123	576
Nr. of Bits	44	611	235	270	123	1283
Group Size	44	306	59	34	4	

TABLE 1. Digest of Signal Flow Data

S/S are given in Table 1, the data repeated from Appendix B. To cut down on the number of words, the specific S/S's of the example will often be referred to as the 40's, 20's etc.

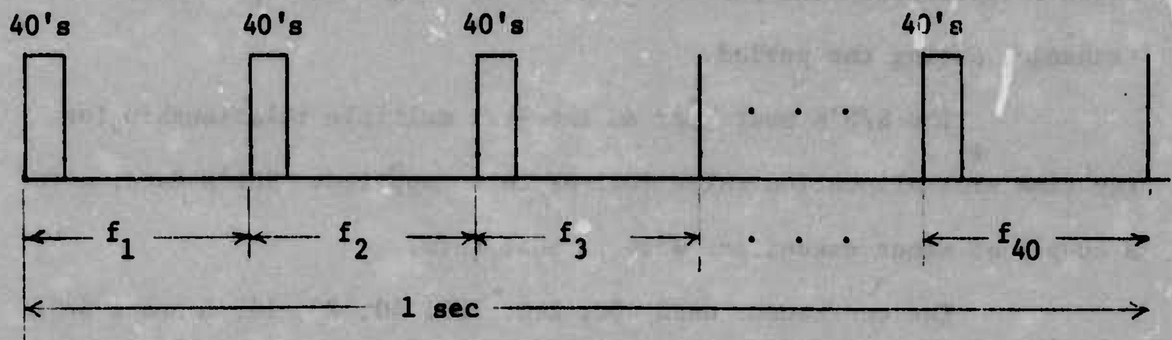

FIGURE 2. Frame Definition

THE PROCEDURE

In the design procedure, the 611 20's bits are divided (as evenly as possible) into two groups, the 235 10's into four groups, the 270 5's into eight, and the 123 1's into forty groups. A standard group size is needed in each category; bits cannot be split, and none can be left over. The group sizes are listed in the bottom row of Table 1. Because the sets of the example did not split evenly, the usual situation, a few void spaces occur on the bus. They are one each in one 20's group, one 10's group, two 5's groups and thirty seven 1's groups. The bus U.F. is over 98%.

FRAME DEFINITION

The highest sampling rate, 40 S/S in our case, defines the frames, see Figure 2. Within the main 1-sec period there are 40 frames,

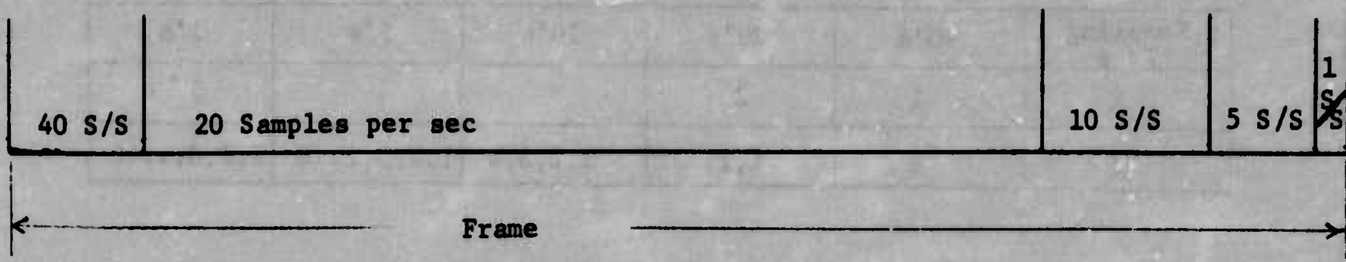

FIGURE 3. A Frame, for the Example, to Scale

labelled f_1, f_2, f_3, . . . f_{40}. The duration of each frame is 1/40 = 25 millisecs.

All the 40's in the system are transmitted first, one terminal after another, at the start of the frames.

The next objective is to fill the remaining space in each frame with the 20's, 10's, 5's and 1's. This is done by putting the two 20's groups, respectively, in frames f_1 and f_2, the four 10's groups, respectively, in frames f_1, f_2, f_3, and f_4, the eight 5's in f_1, f_2, . . . f_8 and the forty 1's in f_1, f_2, . . . f_{40}. The resulting first frame, for the example, is drawn approximately to scale, in Figure 3.

CYCLE DEFINITION

The sequence of bits of the same sampling rate within a frame, is called a cycle. The cycle concept is central to the timing and traffic allocation functioning of the system, and the term will appear often in the report. Since there were 5 sampling rates in the example, there are 5 cycles/frame of different durations, per Figure 3.

CYCLE NOTATION

The following scheme has been set up for labelling the cycles, namely, a two part, or two coordinate, X,Y numbering arrangement.

Sampling Rate	40's	20's	10's	5's	1's
X	1	2	3	4	5
Y	1	1,2	1,2,3,4	1,2,3,...8	1,2,3,..40

TABLE 2. X,Y Cycle Numbering System

The X value is S/S's, per Table 2. X = 1 corresponds to the 40's, X=2 the 20's, etc.

Values of Y are the numbered groups in each category. Y = 1 is the first group in any category, Y = 2 the second, etc.

This two dimensional manner of labelling the cycles permits one to show concisely, the repetitive pattern of the cycles within the main period. It also is convenient for explaining the circuits which achieve some of the timing and control functions later on in the report.

THE CYCLE REPETITIVE PATTERN

Continuing the paragraph titled "FRAME DEFINITION", after appearing in frames f_1 and f_2, the two 20's groups repeat in f_3 and f_4, then again in f_5 and f_6, and so on. The four 10's groups repeat in f_5 through f_8 then again in f_9 through f_{12}. Similarly for the rest of the S/S's and the remainder of the period. This is spelled out in detail in Figure 4. Counting the cycles, using Figure 4 as an aid, it may be seen that there are 55 different ones, 40 of which are needed for the 40 different S/S = 1 groups.

SUMMARY DESCRIPTION; PERIOD, FRAME, CYCLE

An examination of Figure 4 shows that, in the frames, the 40 S/S's, X = 1, appear first in every frame as we have stated, the 20 S/S's (X = 2) repeat after every two frames, the 10's, X = 3, after

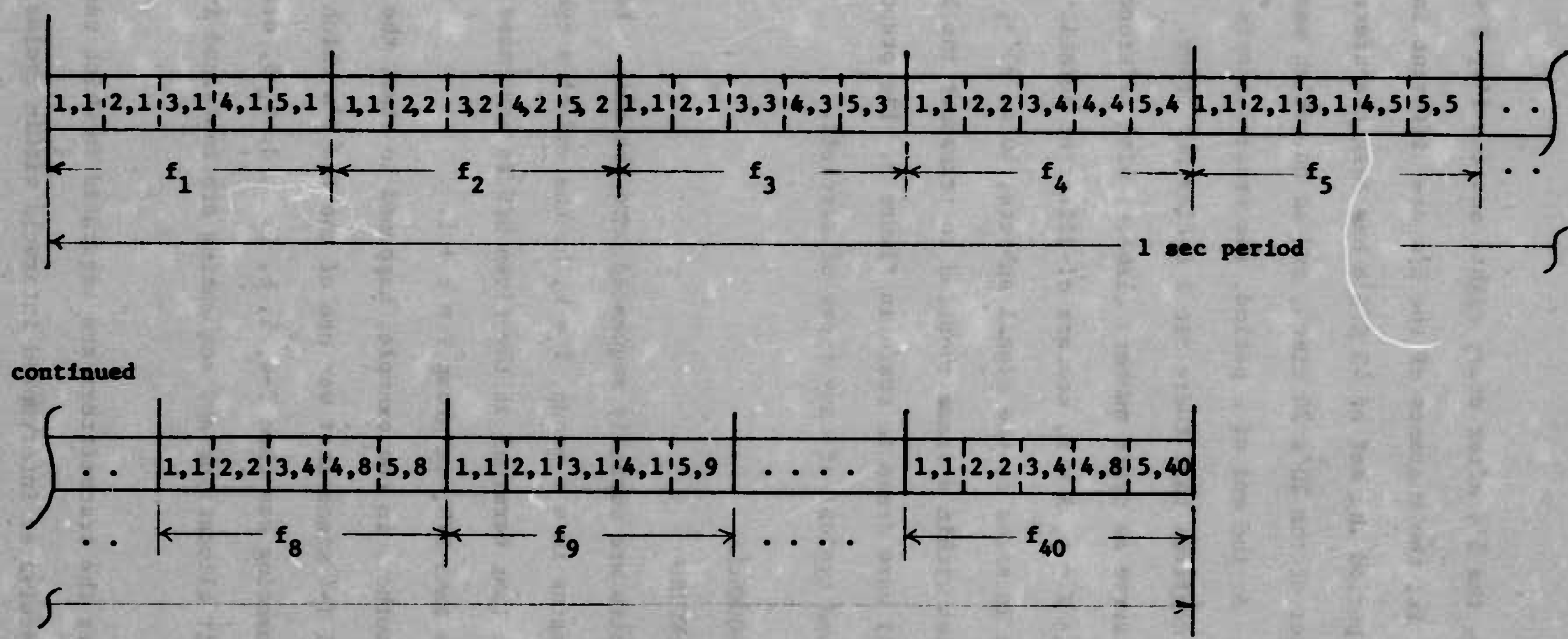

FIGURE 4. The X,Y Cycle Labelling in Detail

every four frames, the 5's after every eight, and the 1's, X = 5, do not repeat. That is, the contents of the 1's are different in every frame. During a period the set of 40 S/S's has been transferred 40 times, every subset of the 20's 20 times, and so on, which was one of the requirements. At the end of a period, the process starts over again. Figure 4 confirms that there are 5 cycles per frame. The values of X also serve as cycle numbers (labels) with reference to the frame. The cycles X = 1, X = 2, etc. are of different durations because of the difference in sizes of the signal subsets, 40's, 20's, etc. The sizes of the cycles within a frame required to transport the bits/cycle (4th row, Table 1) were drawn to scale in Figure 3. The preponderance of 20's is believed typical of many types of aircraft.

III. TERMINAL SEQUENCES

BIT SEQUENCING

The bits are serially sequenced onto the bus by terminal. When no space remains in a Y group, Y = k, at the end of a cycle, transmission from that terminal at the given S/S is continued in the next cycle of the same S/S, in group Y = k + 1.

The author, in the example, happened to start the period off with terminal T-4 since that was one of the two T's which had 40's. The terminal sequencing was then T-4, 5, 6, 1, 2, 3, 4, 5, etc. Details of the bit allocations and sequencing are contained in Appendix B.

Either the transmitters are sequenced in which case some receivers will receive at interrupted intervals within cycles, or the

receivers can be sequenced and the transmitters would have interrupted transmission patterns. Ordering the transmissions was fortuitous, a natural outcome of the way SCI's signal flow tables were arranged.

DIVIDED SAMPLES

Many short sequences of bits on the bus are components of a sample (source reading); either digital numeric originally, or created by a pulse code modulation (PCM) process. One consequence of the design is that in a few cases the bits of a PCM encoded sample will be split into two (or more) frames. It is interesting to note, however, that only in the 1's of the five S/S's is there ever a partial sample delay and hence diminution of sample "freshness" in excess of one frame, or 25 millisecs. In a couple of 1's situations, a sample is spread over several frames. The maximum delay here, however, amounts to less than half the one second sampling interval of that category. It does not seem that this is of practical significance.

IV. TERMINAL ELEMENTS

PRINCIPAL ELEMENTS, Figure 5

The principal terminal elements, from the viewpoint of this report, are (1) a Timing and Control Unit (T & C), (2) Transmitter and Receiver buffer or "scratchpad" memories, CM_T and CM_R, (3) a transmitter and a receiver front end, and (4) a Subsystem Interface Unit, SSIU.

This report is concerned almost exclusively with T & C, CM_T and CM_R. The other elements are shown on the figure, and discussed briefly, to help orient the reader. The SSIU has been mentioned previously. CM_T and CM_R may or may not be part of the SSIU. The front

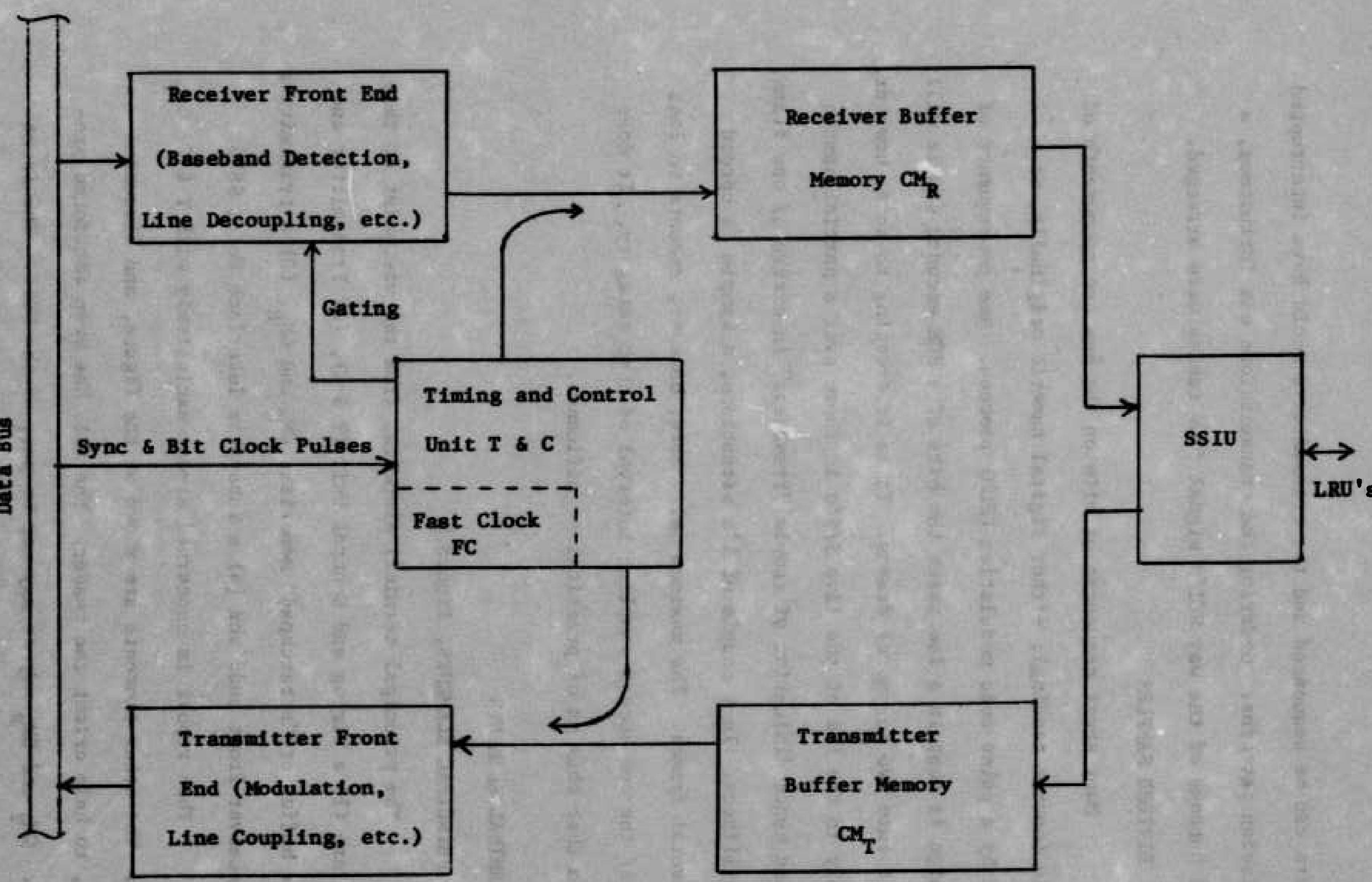

FIGURE 5. Terminal Block Diagram

ends perform the usual functions associated with modulation and demodulation; line coupling and decoupling, Manchester bi-phase level to NRZ conversion and the like. These circuits probably would be similar to those of a comparable Command/Response system as would the SSIU. One possible exception is a control wire from T & C to a gate in the receiver front end. The gate would be operated in synchronization with the arrival of bits destined for the particular terminal, for noise reduction.

TIMING AND CONTROL UNIT, T & C

Each terminal contributes, in a highly self-regimented manner, to the establishment of the bit-time pattern on the bus. Both transmit and receive traffic operations within the terminal are controlled and performed by a single T & C Unit, Figure 5.

T & C

(1) Manages and performs the read out of the avionic signals from CM_T onto the data bus at the proper times, and

(2) Routes incoming signals from the bus in to the proper locations in CM_R.

The curved arrows emanating for T & C in Figure 5 are meant to signify these functions, in a diagrammatic way.

Fast Clock, FC. T & C's primary mode of operation is at the information bit rate, and it is sync'd with the T & C's at the other terminals by synch and clock pulses received from the bus. It does, however, have to perform sets of computer-like operations, each within a fraction of a single bit interval, in connection with five wired-in instructions. These instruction executing operations are sequenced by

a Fast Clock, FC, at a rate of (say) 10 times the bit rate, or in the vicinity of 200 KHz for the example. FC has control lines to most of the components in T & C. A few of these are shown in the component block diagrams, below, for illustrative purposes.

BUFFER MEMORIES CM_T AND CM_R

These are an integral part of the design. That is, bits must be stored in them in patterns compatible with the memory address circuits of the ITS. As temporary memories, they perform a decoupling function between the Timing and Control Unit and the SSIU in the same fashion that buffer memories in leading Command/Response system designs isolate the MTU's and the SSIU's. The same assumption can be made; namely, that the SSIU sampling rate at CM_T can be slightly higher than the ITS data rate in order to assure the availability of fresh samples at all times.

V. TIMING AND CONTROL UNIT COMPONENTS

THE COMPONENT LIST

Transmitter Bit Selector TBS

Begin Transmit/End Transmit Timer BT/ET

Time Cycle Counter TC

Cycle End Circuit CE

Cycle Designator X,Y

Receiver Address Unit RAU

Begin Receive/End Receive Timer BR/ER

Fast Clock FC

OVERVIEW OF T & C COMPONENT OPERATION

T & C's tasks are to achieve the proper memory to bus and bus to memory transfers. Although they are never simultaneous on a bit basis, from a less exact standpoint, these are parallel operations. On the components list, the first two items are concerned solely with transmission and the sixth and seventh solely with reception. The remaining items participate in both functions, on a shared basis.

Memory address and memory information registers, closely allied to the Transmitter Buffer Memory, CM_T, and the Receiver Buffer Memory, CM_R, have been arbitrarily lumped into the T & C Unit.

Although not "T & C Components", CM_T and CM_R play important roles in the discussions which follow.

"Where" and "When" Guideposts. Every bit has a precise predetermined location in the CM_T of one terminal and the CM_R of another terminal. It also has a precisely defined position on the time scale when it is transferred over the bus. The vital matter of bit identification can be broken down into two simple parts, "where", and "when". The Transmitter Bit Selector, TBS, and the Receiver Address Unit, RAU, are concerned with "where" (in memory), see Figure 6. The Begin Transmit (Xmt)/End Xmt Timer, BT/ET, and the Begin Receive (Rcve)/End Rcve Timer, BR/ER, are concerned with "when" (on the line). The remaining components assist in both where and when determinations.

Measuring Time. Time is measured in the terminals by counting bit clock pulses from a reference point in time, which is the once-per-period sync pulse on the bus. The count is kept in such a way that both present (current) cycle, X,Y, and current bit within the

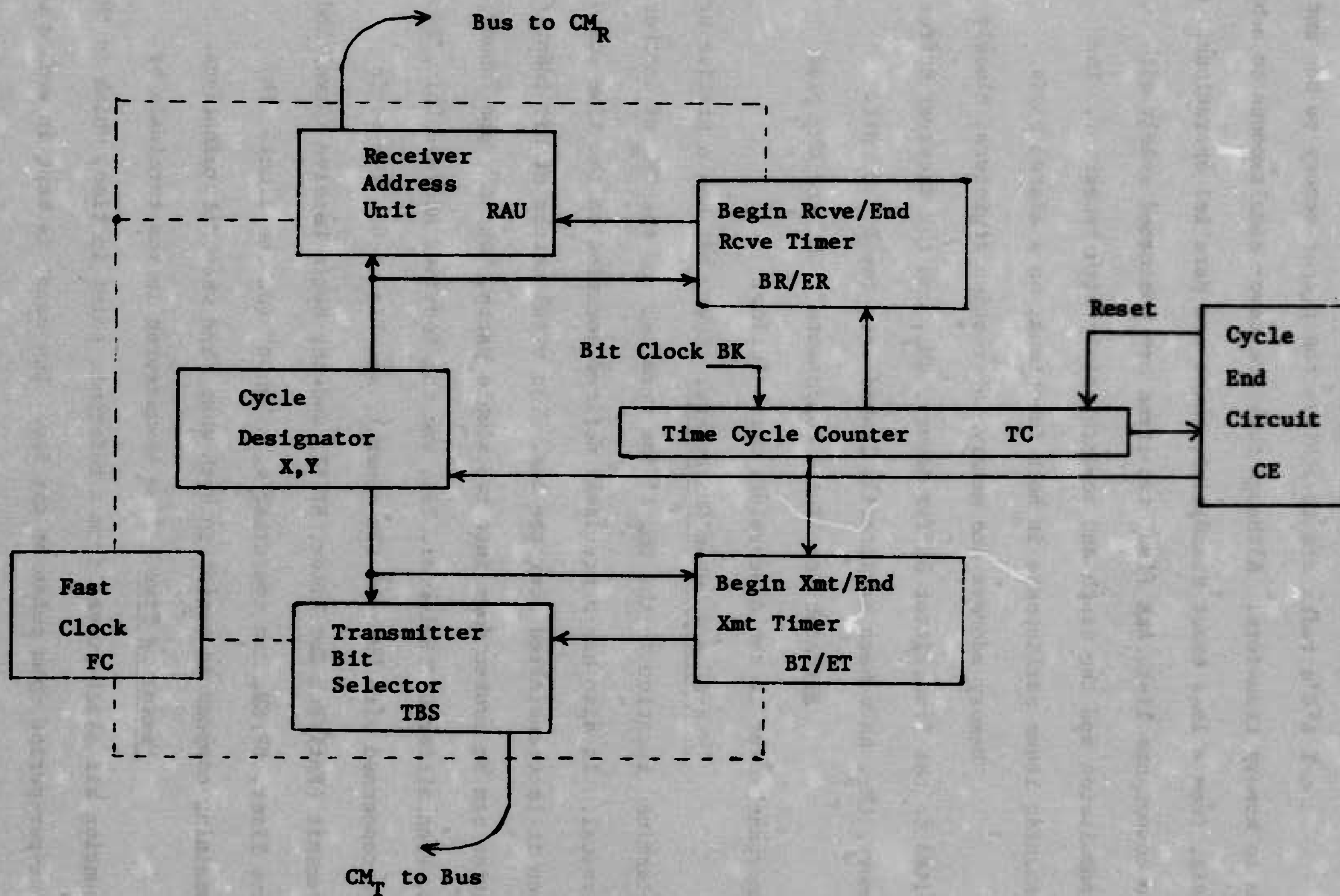

FIGURE 6. Timing & Control Unit T&C

cycle are known. Although present frame is also available as an implicit function in the circuitry, it has no direct application in the operation. The value of the "frame" concept has been as an aid in explaining the bit allocation scheme on the bus, and the repetitive cycle pattern, X,Y.

Cycle Designator X,Y. X,Y's functions are to determine and indicate the current cycle, X,Y. ("X,Y" is used in the report, to denote, interchangeably, (1) the Cycle Designator Unit, (2) its outputs, and (3) later on, the location in memory that the X,Y value addresses.) The X,Y outputs (see Figure 6) connect to

(1) The Receiver Address Unit, RAU, and the Transmitter Bit Selector, TBS, because the related addresses in CM_R and CM_T, respectively, are functions of X,Y, and

(2) Begin Rcve/End Rcve, BR/ER, and Begin Xmit/End Xmt, BT/ET, because the exact points in time during the cycle when receptions and transmissions are to occur are also functions of the cycle, X,Y.

Time Cycle Counter TC. TC counts bits from the start of the cycle. That count, provided to BR/ER and BT/ET, permits those units to signal to RAU and TBS the exact moments these latter circuits are to time information onto and from the bus.

Cycle End Circuit CE. CE plays a dual role. It

(1) resets TC to zero at the end of each cycle, and

(2) provides an output pulse to X,Y at each reset so that X,Y can count cycles thereby determining current cycle.

Stored Data for Instructions. The operations performed by the eight T & C Components are digital computer-like in nature. Because of their limited number and simplicity, the instructions are permanently wired into the terminals. The traffic management data used in the operations consist of (1) addresses in CM_T and CM_R, (2) start and stop transmit and receive epochs, and (3) cycle lengths. CM_T and CM_R are indirectly addressed, and indirect addressing is used in the begin receive, end receive operations, to reduce required memory space. The assumption was made that the number of sampling rates can be standardized (5 were used in the scaled down example). The number arrived at would, in effect, be wired into the circuitry. The cycle length numbers are the same at all terminals. The other sets of numbers, or operands, are different at every terminal. All the operands depend on the particular avionics suite in the aircraft. They are on plug-in memories as previously explained. All operand values required in the example have been tabulated in Table 1, 4th row, and in Appendix B, Tables B-5 and B-6. These will be referred to in more detail, later on.

Fast Clock FC. FC, using command wires to the applicable components of T & C, sequences the instruction steps of the previous paragraph in the proper orders.

VI. TIMING AND CONTROL COMPONENTS (DETAILED)

TRANSMITTER BIT SELECTOR TBS, Figure 7

The TBS consists of (1) a Transmit Control Unit, TCU, (2) a Start-Address Memory, SA_T, (3) a Memory Address Counter, MA_T, and (4) a

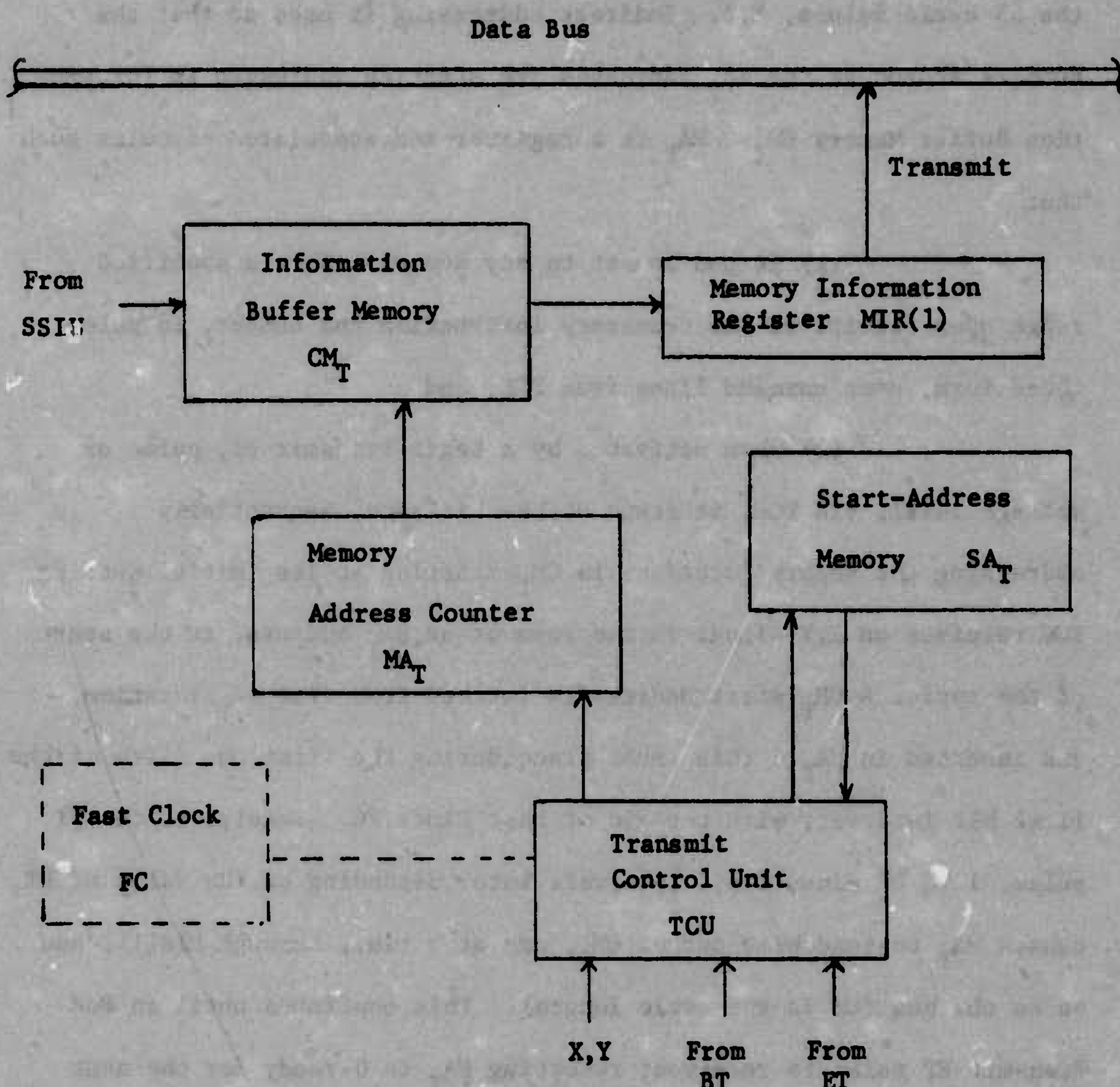

FIGURE 7. Transmitter Bit Selector (With the Info Memory)

one bit Memory Information Register, MIR(1).

Operation: TCU receives command signals from X,Y and BT/ET. SA_T contains 55 hardwired memory locations, corresponding to the 55 cycle values, X,Y. Indirect addressing is used so that the numbers stored at the SA_T addresses are starting addresses in Information Buffer Memory CM_T. MA_T is a register and associated circuits such that

(1) it can be set to any number within a specified range upon receipt of the necessary instruction and number, in pulse coded form, over command lines from TCU, and

(2) when activated by a Begin Transmit BT, pulse or voltage level, via TCU, it steps at the bit rate, sequentially addressing the memory locations in CM_T starting at its initial setting. TCU receives an X,Y signal in the form of an SA_T address, at the start of the cycle. A CM_T start address is fetched from that SA_T location, and inserted in MA_T. This takes place during the first one fifth of the first bit interval, with the aid of Fast Clock FC. Receipt of the BT pulse, 1 to CE minus 1 bit intervals later depending on the value of BT, causes MA_T to read bits out of CM_T, one at a time, through MIR(1), and on to the bus (CE is the cycle length). This continues until an End Transmit ET pulse is received; resetting MA_T to 0 ready for the next cycle, and terminating the process.

Bit Storage in CM_T. The bits to be transmitted from each terminal, T, are stored sequentially, one bit per location, in an arbitrary order, in that T's CM_T. The addresses, for purposes of explanation; are numbered consecutively, 1 to x. x is a number of

memory locations provided sufficiently large to accommodate all of the bits of the terminal including any conceivable retrofit additions. Of this list, the predetermined start locations of the cycle and terminal, are stored in SA_T. For the A-10 example, these numbers are given in Table B-5, which also gives the values of BT and ET. The last column in Table B-5 labelled CM_T, lists in parenthesis the number of bits read out during the transmission, and, as a subscript, the number of the terminal to which the bits are directed. These numbers relate back directly to SCI's basic signal flow data. They were used in the construction of the table, and are included for completeness.

An Illustration. Let the transmitting terminal be T-2, and the cycle be X,Y = 3,2. From Table B-5, the start address in CM_T, stored in SA_T, is "address No. 64". Starting on bit count 25 measured from the start of the cycle and ending on bit count 60, 35 bits are transmitted to terminal T-3.

It may be noted from Table B-5, that for many cycles, there are no transmissions from a given terminal. In these cases a 0 is stored in SA_T and the operation stops at the reading of that zero.

MIR(1), which feeds bits to the bus, is viewed as an isolator or buffer, inserted for pulse fidelity reasons and not basic to an understanding of the system operation.

SSIU Compatibility. The compatibility requirement with the SSIU is that it puts the bits in the CM_T locations in which the ITS will look for them.

BEGIN TRANSMIT/END TRANSMIT TIMER BT/ET, Figure 8.

BT/ET specifies to Transmitter Bit Selector, TBS, the times

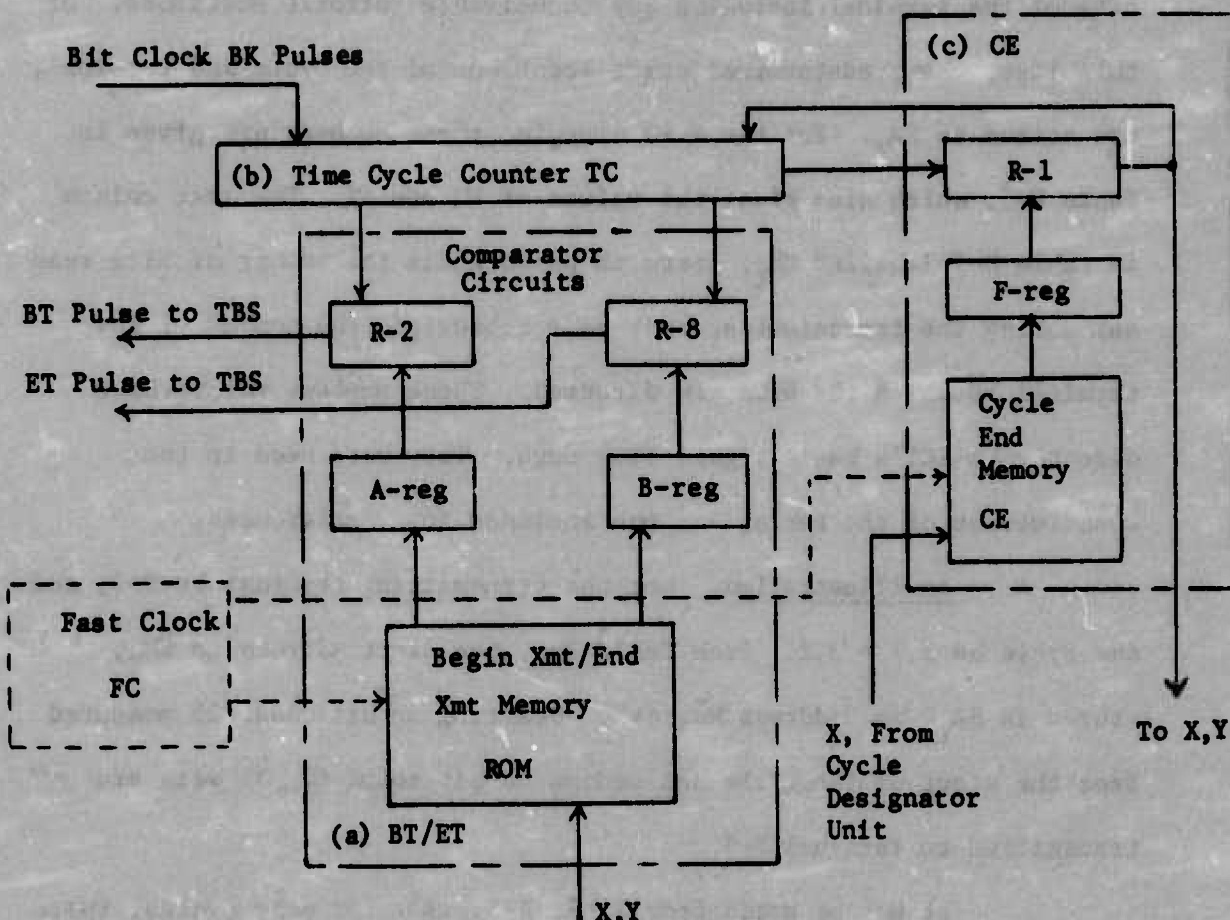

FIGURE 8. (a) Begin Transmit/End Transmit Timer, (b) Time Cycle Counter, (c) Cycle End Circuit

to start and stop transmissions on the bus. It consists of

(1) a read only memory (ROM) with its read circuits,

(2) two comparator circuits each consisting of a recognition gate and a temporary storage register; one circuit for BT and the other for ET.

Its inputs are (1) the X,Y addresses from Cycle Designator X,Y, and (2) the current count, in bits, with respect to the start of the X,Y cycle, from Time Cycle Counter TC.

Within the ROM there are 55 hardwired addresses corresponding to the 55 possible values of X,Y. At each address and the memory location which follows it, proper BT and ET values, respectively, are stored. These would be precomputed for the entire system along with the operand values for the Transmitter Bit Selector, the Cycle End Circuit, the Receiver Address Unit, and the Begin Rcve/End Rcve Timer as one exercise probably with the aid of a special ground computer program. The operand values would be "burned in" to the plug-in ROM's before the aircraft is delivered. Values for the A-10 example are contained in Table B-5.

The recognition gate is a two-input, one-output device which outputs a pulse when the numerical values of its two inputs are equal. It forms the logic function $Y = \bar{A}B + A\bar{B}$ where A and B are the respective inputs. The two inputs to each gate are the TC bit count and the stored number; BT for one gate and ET for the other. When TC reaches the count in the A-reg, Figure 8, Recognition Gate R-2 sends a BT pulse on a command wire to TBS. When TC reaches the count in the B-reg some number of bits later, coincidence occurs in R-8 and an ET

pulse is sent to TBS. R-8's output also resets the A and B registers to 0, ready for the next cycle.

As with the TBS, previously explained, and with many of the T & C Components which follow, the fetch-from-memory, place-in-register and other computer operations are executed rapidly during the first portion of the first bit interval of the cycle, under the aegis of the Fast Clock FC. Here, for example, the FC circuit might contain a flip-flop to read BT and ET from the ROM in sequence.

As with TBS and the analogous receive operations described later on in the report, when there is no transmission (or reception) at the terminal during the cycle, a 0 is stored in the memory, terminating the computer operation at that point.

TIME CYCLE COUNTER TC, Figure 8

This unit is relatively simple, and already has been referred to several times. It is a counter type register, capable of counting up to the highest number of bits in a cycle that would be encountered in the aircraft, or class of aircraft in which it is installed. Its operation is simply to count the incoming clock pulses, at the bit rate, up to the number of bits which constitute the length of the particular cycle it is counting.

In spite of its comparative simplicity, it is given status on the T & C Component list because of its extreme importance to the operation of the Timing and Control Unit. It both

(1) directly provides the times for the starts and stops of the transmit and receive operations within the cycles as previously explained, and

(2) with the aid of its auxiliary circuit, the Cycle End Circuit CE, provides the means for counting cycles, and hence identifying the cycles, to the Cycle Designator X,Y.

CYCLE END CIRCUIT,CE, Figure 8

This is also a relatively simple unit, closely allied to Time Cycle Counter TC. It is listed separately as a Component of T & C because of its importance and the fact that it is one of the five elements wherein data vital to the operation of the terminals must be stored. Its operations are (1) to reset TC to zero at the end of each cycle at bit counts and hence relative times which accord with operands stored in CE's memory, and (2) in the process, emit a cycle count pulse on a command line to Cycle Designator X,Y. (X,Y, by counting these keeps track of the cycle the system is currently operating in.)

CE consists essentially of (1) a Recognition Gate R-1, (2)a temporary register, F-reg, and (3) a plug-in memory module with five addresses wired to respond to the five values of X. See Table 1, 4th row. That is, the five cycle lengths needed to handle the bits of the five sampling rates are preset when the aircraft is delivered. They can be changed on the ground later if the avionics complement is modified. Note that the memory requirements here (1) are much less than for the other four T & C components where operational storage is required, and (2) they differ from those, also, in that the set of numbers is the same at every terminal, rather than a different set for each terminal.

<u>Operation</u>. The coded signal X addresses a location in CE's memory and fetches the cycle-end number stored there, into the F-reg. Here that value is compared continuously with TC's count in R-1 until

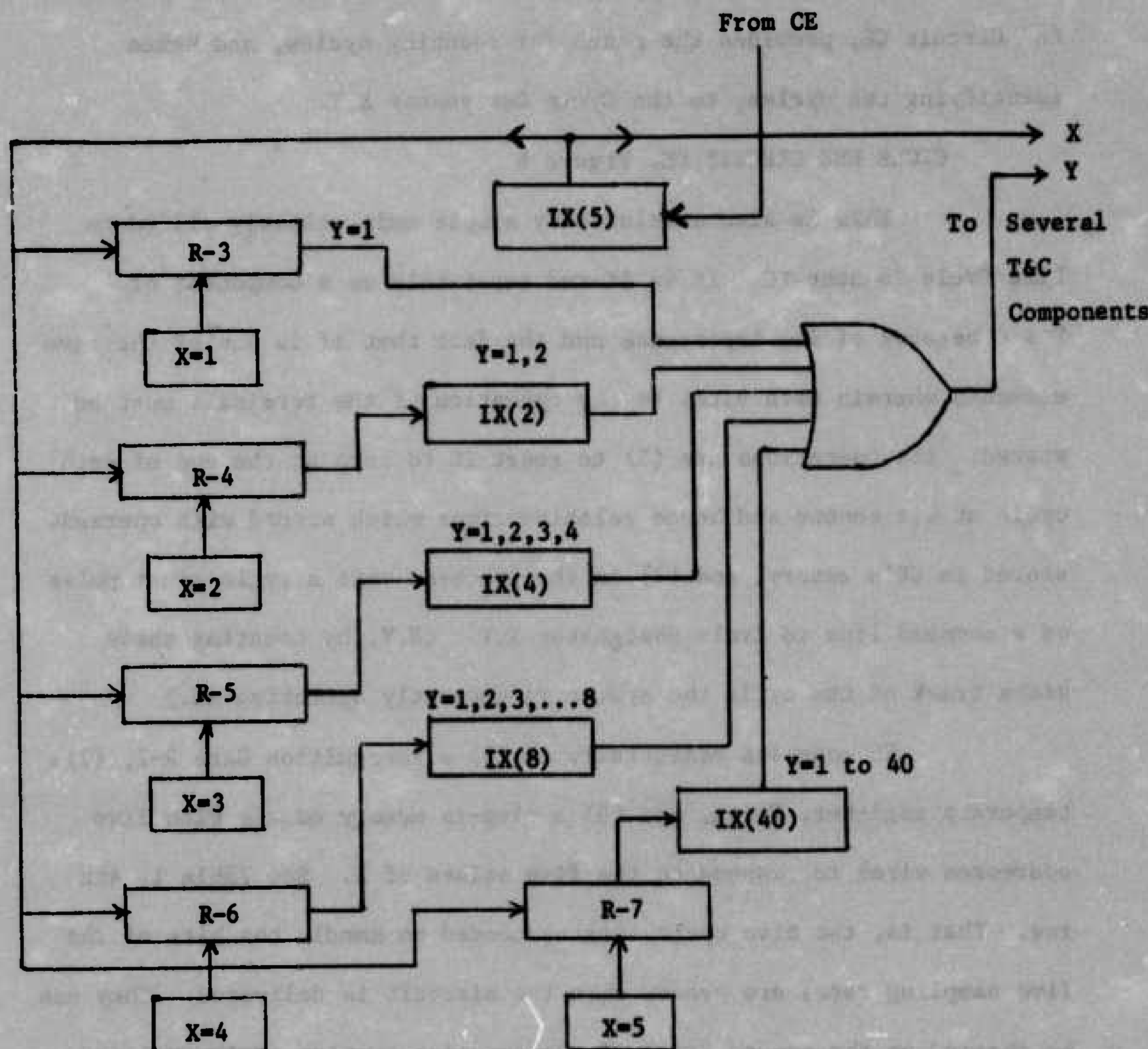

FIGURE 9. Cycle Designator X,Y

coincidence is reached. At that point in time, an output pulse from R-1 resets TC to 0 and forwards a count pulse to X,Y.

CYCLE DESIGNATOR X,Y, Figure 9

This pivotal T & C component keeps track of the current cycle, and distributes that number in coded form over command lines to several other T & C units.

Including repeats, there are 5 cycles/frame x 40 frames = 200 cycles in a period. Fifty-five different cycles, appearing in the rather peculiar repetitive pattern of Figure 4, make up this 200 total. It is the task of X,Y to create that timing pattern as operation progresses through a main period.

Inputs to X,Y are (1) the sync pulse from the bit clock which identifies the start of each period, and (2) the cycle-end pulses from CE, which are counted from the start of the period. Keeping this count provides identification of the cycles.

X,Y's output transfers directly to the Transmitter Bit Selector, the Receiver Address Unit, the Begin Transmit/End Transmit Timer, and the Begin Receive/End Receive Timer.

Description. X,Y consists primarily of (1) one index register, IX (5) which counts the values of X, [i.e., the numbers 1 through 5, frame after frame, without regard to which specific cycles (of the 55 possible ones)] that they consist of, (2) four index registers, IX (2), IX (4), IX (8), and IX (40) which count, respectively (and then repeat) Y = 1, 2, Y = 1, 2, 3, 4, Y = 1, 2, . . . , 8, and Y = 1, 2, 3, . . . 40, (3) five recognition gates, R-3 through R-7, (4) five stored values, X = 1 through X = 5, and (5) an OR gate.

Operation. The elements are interconnected as shown in Figure 9. Assume an initial condition, at the start of the main period, of all indexers set to zero. The five Recognition Gates, connected in parallel, compare IX (5)'s count with the respective associated and stored values 1 through 5. On the count X = 1, (the 40 S/S's) in every frame R-3 outputs a Y = 1 pulse. The first time that IX (5) emits a 2 in the period, i.e., at the start of the second cycle in frame f_1, the coincidence pulse from R-4 causes IX (2) to emit Y = 1 to the OR gate, and step to its own count of 2 and wait. When the IX (5)'s output is a 2 the next time around, which is the start of the second cycle in f_2, R-4's output pulse causes IX (2) to output Y = 2 to the OR gate, and reset to 1. The operation of the remaining circuits is exactly the same except that the Y counts extend to higher values before repeating.

The X-component of the Cycle Designator's output is taken directly from IX (5) as shown in the figure. Values of Y are out of the OR gate, and have been matched properly with values of X by the process described. Thus the repetitive X,Y pattern required is produced as operation progresses, with time, through the main frame.

RECEIVER ADDRESS UNIT RAU, Figure 10

RAU consists of (1) a Receive Control Unit, RCU, (2) a Start-Address Memory, SA_R, (3) a Memory Address Counter, MA_R, and (4) a one bit Memory Information Register, MIR(2).

In a manner similar to the way Transmitter Bit Selector TBS received its "instructions" from X,Y and BT/ET, RCU receives commands from X,Y and BR/ER. SA_R has 55 memory locations wired to be addressed

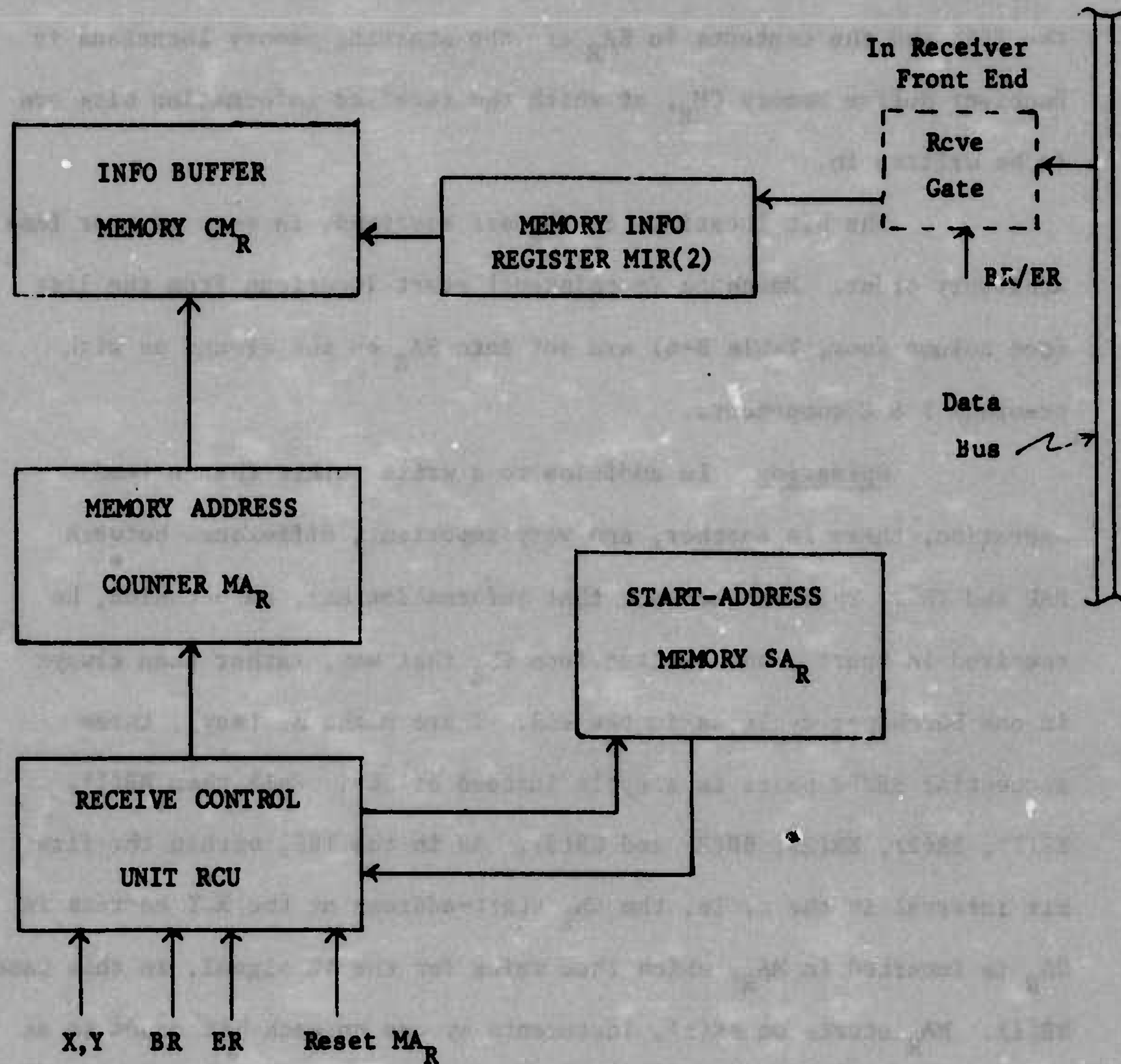

FIGURE 10. Receiver Address Unit RAU (with the Receive Info Memory Unit)

by the 55 values of X,Y. Indirect addressing is employed as it was in the TBS; and the contents in SA_R are the starting memory locations in Receiver Buffer Memory CM_R, at which the received information bits are to be written in.

The bit locations in CM_R are assigned, in some more or less arbitrary order. Matching (consistent) start locations from the list (see column four, Table B-6) are set into SA_R on the ground as with previous T & C components.

Operation. In addition to a write rather than a read operation, there is another, and very important, difference between RAU and TBS. That is the fact that information may, on occasion, be received in spurts, and written into CM_R that way, rather than always in one batch per cycle as in the TBS. There might be (say), three sequential BR/ER pairs in a cycle instead of one. Call them BR(1), ER(1), BR(2), ER(2), BR(3) and ER(3). As in the TBS, within the first bit interval in the cycle, the CM_R start-address at the X,Y address in SA_R is inserted in MA_R, which then waits for the BR signal, in this case BR(1). MA_R starts on BR(1), increments by one on each bit count so as to write into consecutive address in CM_R, then stops on ER(1). It cannot, however, reset to 0 as in the TBS, for there is more work to be done. It maintains its place in CM_R until started again by BR(2), stopped by ER(2) etc. Finally, after ER(3), known at BR/ER to be the final end-receive of the cycle, a "reset MA_R" pulse is sent from BR/ER to the Receiver Control Unit, on a separate command wire. This terminates the operation of the Receiver Address Unit for the cycle.

BR/ER signals also open and close a gate in the front

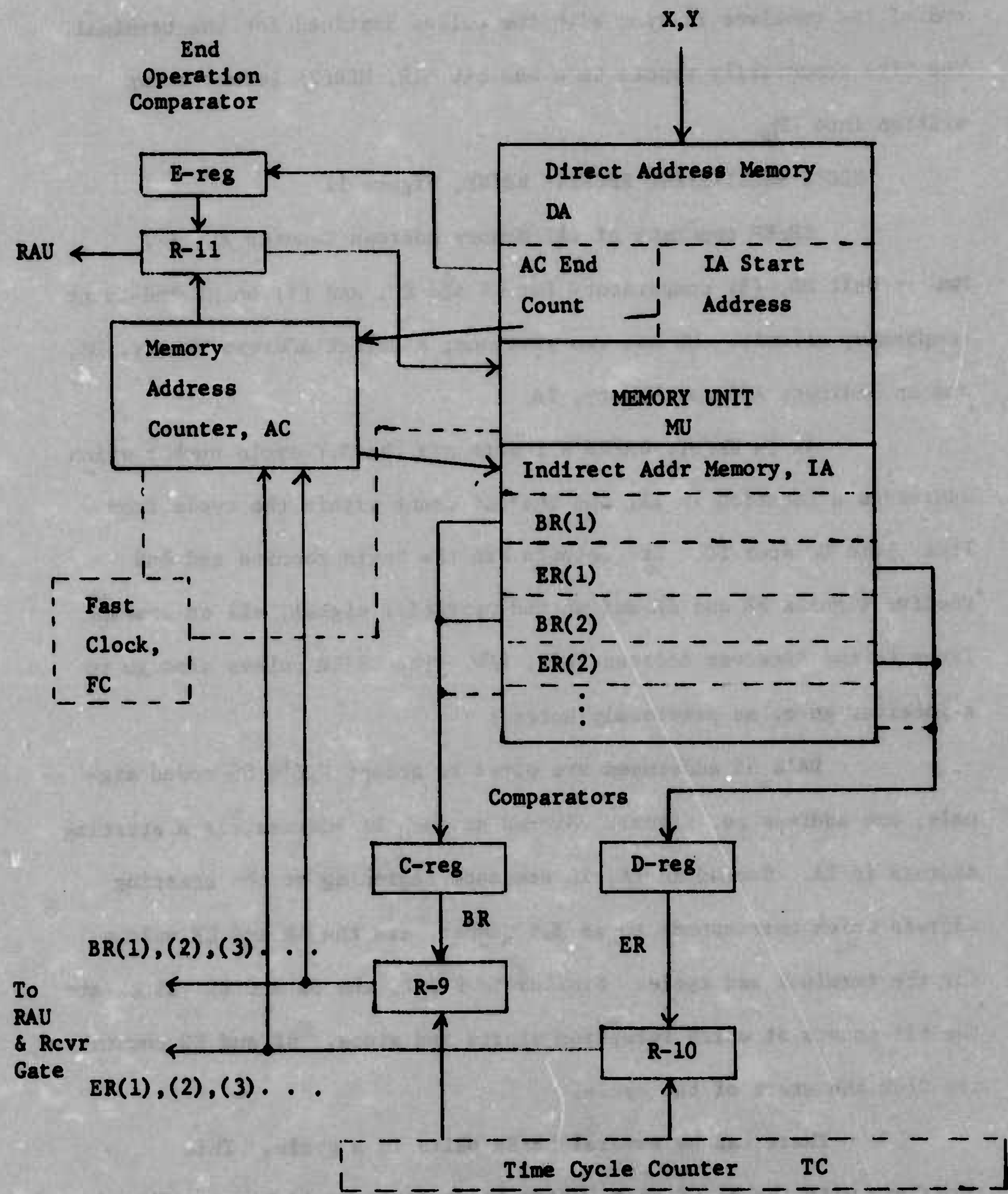

FIGURE 11. Begin Receive/End Receive Unit BR/ER

end of the receiver in sync with the pulses destined for the terminal. The bits temporarily repose in a one bit MIR, MIR(2) before being written into CM_R.

BEGIN RECEIVE/END RECEIVE BR/ER, Figure 11

BR/ER consists of (1) Memory Address Counter AC, (2) Memory Unit MU, (3) comparators for BR and ER, and (4) an AC End-Count comparator circuit. MU has two sections; a Direct Address Memory, DA, and an Indirect Address Memory, IA.

As in BT/ET, BR/ER's inputs are the X,Y cycle number which addresses a location in IA, and the bit count within the cycle from Time Cycle Counter TC. Its outputs are the begin receive and end receive signals BR and ER and an end operation signal, all on command lines to the Receiver Address Unit, RAU. (The BR/ER pulses also go to a receiver gate, as previously noted.)

DA's 55 addresses are wired to accept X,Y's 55 coded signals, one address per signal. Stored at each DA address, is a starting address in IA. Stored in IA, in sequence beginning at the starting address which corresponds to an X,Y number, are the BR and ER values for the terminal and cycle. Similar to BT/ET, the BR and ER values are the bit counts at which reception starts and stops. BR and ER counts are from the start of the cycle.

There can be several BR/ER pairs in a cycle. This contrasts with the BT/ET unit, where there never would be more than 1 pair per cycle. BR and ER are alternated in IA's sequential locations, as shown pictorially in the figure for two pair: BR(1), ER(1); BR(2), ER(2). The probability that there will be multiple pairs in some

cycles, is the reason for this second level indirect address feature. Part of the design philosophy is that there be no need to try to predict into which cycles the particular avionic suite will "throw" multiple values of BR/ER. With this arrangement IA is made large enough to handle the largest total signal set that might be encountered, without regard to how the interrupted receptions at terminals are distributed. The purpose of the second level indirect addressing is to make efficient use of memory space.

The actual BR/ER numbers are determined by the succession in which the transmitted bits were ordered onto the bus. The BR/ER values for a particular system would be tabulated, by cycle, and by terminal as has been done in Table B-6 for the example. They would be loaded in cycle sequence into the ROM's, IA, before the aircraft is delivered. The corresponding IA start addresses would be loaded into the ROM's DA.

AC steps through the BR/ER pairs in IA, and with the aid of FC, arranges their transfers into the BR and ER comparators. AC must be stopped and reset to 0 when it has stepped through the number of pairs associated with that cycle, at that terminal. Also, an end operation pulse must be sent to RAU only after the final ER count has been reached. Both of these functions are achieved by allocating three bit spaces at each DA address to an AC end count number, and providing an end-operation comparator circuit, Figure 11. Their operation is explained in the next paragraph.

<u>Operation</u>. Consider the two BR/ER pair example in the figure. A number equal to twice the number of pairs, or 4, has been

set in the AC End Count space in DA. AC steps only when pulsed by the BR or the ER comparator. The AC End Count number is transferred to temporary register, E-reg. The number of times AC has stepped is output to the Recognition Gate, R-11. At the start of the cycle the IA start address is transferred to AC, and BR(1) is placed in the C-reg. In what follows, symbols in brackets such as (TC) means "the contents of". When (TC) = (C-reg) which is BR(1), a BR pulse is output from R-9 to RAU and to AC stepping it one address from BR(1) to ER(1) and placing ER(1) in the D-reg. AC now waits until (TC) = (D-reg) which is ER(1) whereupon an ER pulse is output from R-10 to RAU and to AC stepping it from ER(1) to BR(2) and placing BR(2) in the C-reg. AC waits until (TC) = (C-reg) which is BR(2) whereupon a BR signal is output from R-9 to RAU and to AC stepping it from BR(2) to ER(2) and placing ER(2) in the D-reg. AC waits until (TC) = (D-reg) whereupon an ER signal is output from R-10 to RAU and to AC. FC's fast timed logic is sequenced so that AC's step-count pulses to R-11 occur before AC steps to the next address in IA. AC has now been stepped 4 times, which is the AC end count in the E-reg. R-11's resulting coincidence output inhibits the remainder of AC's normal cycle (i.e., prevents AC from stepping to the next address in IA), and, instead, resets AC to 0, ready for the next cycle. R-11 also outputs a pulse to RAU on a separate command line which resets the Memory Address Register MA_R in that unit, to zero. The same procedure extends to a larger number of BR/ER pairs. The largest number of separate receptions during a cycle for the A-10 example was 5 at T-4 during cycle number 2, 2, see Table B-6.

Illustrative Example. Let the receiving terminal of interest be T-2, and the cycle be 4,2. From the column headed CM_R in Table B-6 it is seen that 26 bits will be received from T-4 and 3 from T-5. The 26 from T-4 arrive during the first 26 bit intervals of the cycle. The 3 from T-5 arrive starting at bit interval 30. Reading from the columns headed BR and ER, BR(1) = 1, ER(1) = 27, BR(2) = 30, ER(2) = 33. At each terminal, the alternating BR and ER values are stored and numbered in the order in which they appear in Table B-6. The IA start address numbers appear in the columns headed IA. For the illustration, the IA start address number stored in DA's memory location addressed by an incoming cycle number X,Y = 4,2, is 11. The AC end count number is 4.

FAST CLOCK FC

Time has not permitted an exploration of this important and fascinating area in any depth, which fact is regretted. Therefore, the comments on this item must be general.

It appears from a cursory examination of computer literature, that the conventional implementation might be a bistable clock as a pulse source, a ring counter, and a large number of command lines and logic gates distributed about the Timing and Control Unit T & C. A claimed advantage of ring counters over other types of counters for timing the execution of instructions in a computer is that each count comes out on a different line from the counter. This permits direct wiring to the various elements in combinational logic networks and supposedly results in less total logic.

The Fast Clock operations must be performed at the right

times with respect to the bit timing, usually within the first part of the first bit interval in each cycle. Possibly this could be effected by providing a positive step of voltage as bias, from the bit rate circuits, to start the pulse source coincident with the cycle starts. The ring counter would also have to be reset to the same starting point after every sequence of instruction executions. This is because the sequence in which the pulses are emitted from the "hardwired" ring counter over different leads is the important thing; and the start has to be at the same wire for each repeat of the sequence of program executions. With this arrangement it would not be necessary to synch the FC's to the Bit Clock BK.

The exact FC frequency does not appear to be at all critical. Its upper limit might be the reaction time of the logic gates in the network, which would be several MegaHertz. It must be fast enough to perform several computer instructions in a fraction of a bit interval. This will take care of the worst case where a bit must be transferred into or out of memory in the same bit interval that the instruction is executed. The lower practical frequency limit might be somewhere between 200 KHz and one MHz. It follows that

(1) The FC's at the different terminals do not have to be adjusted precisely to the same frequency. This is an attribute to a federated system.

(2) The stability of each FC does not have to be particularly high. It would appear that it only need to be high enough so that deleterious transients are not generated by frequency fluctuations.

In view of the above it appears that FC could be a relatively inexpensive item.

VII. BIT CLOCK BK

DISCUSSION

BK provides the basic timing signals to all terminals for the proper synchronous operation of the system. It should be located at a point accessible to the bus, close to the center of the fore and aft line of the aircraft, to minimize the effect of clock skew. BK impresses a square wave onto the bus, at a frequency of 17,880 Hz, which is slightly higher than the 17,803 bps bit rate of the system.

It is probable that the clock pulses will be carried on a separate wire in the bus. However, to simplify bus construction the possibility of also transmitting clock on the same twisted wire pair as the information will be considered.

The frequency of BK must be made adjustable, so that it can be set to match the avionics suite and its signal list when the aircraft is delivered. It also would be readjusted if any retrofit change of any importance were made later on. The accuracy to which it can be set need not be at all high. This is because any set of standard sampling rates agreed upon would be rather arbitrary. Whether the 40 S/S rate was that, or 43 S/S, for example, a difference of almost 10%, would appear to be of no practical significance. Frequency stability requirements also should be moderate, just so there are no changes rapid enough to cause deleterious transients. For slow frequency fluctuations, the whole system drifts as a unit without creating any obvious problem.

(If one of the users of the ITS is a computer, this matter would have to be examined carefully.)

The sync pulses occur once a second regardless of the clock repetition frequency. They are to be generated independently and added to the output of the basic clock. This way, the clock rate can be varied without changing the interval between sync pulses.

VIII. FUTURE DEVELOPMENT

The trend is toward the use of airborne computers even for smaller, less elaborate aircraft. Many of the computer functions are purely computational; and it would be desirable that sensor outputs be provided to them in a format which can be used directly. To that end, signal conditioning could be performed at the terminals, which development approach is consistent with the distributed traffic management design philosophy of the cooperative terminal ITS.

It would appear that simple pre-processing functions could be accomplished by elementary microprocessors without unduly complicating the remote terminal design. Such processors, operating under firmware control within the terminals, could relieve a computer of routine functions.

As pointed out in (5), page 219, examples of pre-processing in a "smart" terminal include the performance of data compression by the logical combination of two or more input signals to form a single data output required by a general purpose computer.

(5) "Standard Multiplex Interface Definition for Advanced Aircraft Avionics", AFAL-TR-74-132, Vol. I, Contract F33615-73-C-1222, SCI Systems, Inc., July 1974.

IX. CONCLUSIONS

The primary application of this new time division information transfer system (ITS) is to small and medium size USAF aircraft of low or moderate sophistication. The RPV and the A-10 are mentioned as possible applications.

For those aircraft, the cooperative terminal internal data distribution system described in the report probably would be considerably simpler than a multiplex system built in conformance with MIL-STD-1553 (USAF), (1).

The greater simplicity should result in greater dependability and lower cost of ownership. It is due to:

(1) Elimination of the central bus controller plus the considerable amount of hardware in the terminals associated with the Command/Response mode of the Mil Std.

(2) Operation of the bus at a much lower frequency.

It is possible to run the bus at a much lower frequency than 1 MHz by:

(1) Doing away with the supervisory (traffic control) words on the bus.

(2) Eliminating the standard information word format with its attendant poor signal packing factor for small and intermediate complexity aircraft where the signal sets are relatively small.

(3) Achieving a very high bus utilization factor by means of a bit allocation scheme on the bus which is unique for this internal aircraft multiplex application.

(4) Recognizing that the signal sets are much smaller and hence

the signal requirements are much lower for smaller and lower performance aircraft.

It is believed that the design proposal to utilize replaceable (plug-in) memories for the storage of the system operating parameters will permit a high degree of circuitry standardization in the Multiplex Terminal Units (MTU's). This feature, plus the much lower bus frequency which alleviates signal deterioration due to wide band line and stub impedance matching problems, are the bases for the claims of probable greater simplicity and reliability and lower total cost of ownership.

Three standard bus transmission rates might be set up; (say) 1 MHz for large and high performance aircraft, 250 or 500 KHz for medium performance, medium size aircraft, and 50 or 100 KHz for small aircraft.

The cooperative terminal ITS has some of the attributes of a central control system and some of those of a federated or distributed processor system. As such, it may serve as a reference against which the expected performance of other technical approaches can be compared later on.

It is concluded that:

(1) The approach described in the report shows sufficient promise to warrant an in-house experimental hardware and computer simulation program to verify its utility.

(2) The design description is sufficiently detailed that work could start immediately in the preparation of a test plan and the procurement of necessary components and subassemblies.

X. RECOMMENDATIONS

A combined breadboard and computer simulation laboratory program is recommended. The PDP-10 or one of the PDP-11's could be used to simulate the avionic signal set of an A-10 aircraft. Integrated circuits and solid state subassemblies could be combined to approximate the terminals described in the report.

Hopefully, the test plan would keep the RUSMUX in mind, so as to be supportive of a Command/Response - Cooperative Terminal - RUSMUX quantitative comparative evaluation at some later date.

REFERENCES

(1) Military Standard "Aircraft Internal Time Division Multiplex Data Bus", MIL-STD-1553 (USAF), 30 Aug 1973.

(2) "A New Data Distribution System for Aircraft", AFAL-TR-73-133, Blinn W. Russell, July 1973.

(3) "The Application of Information Transfer Techniques for Solving the Internal Communication Requirements of a Night AX Aircraft", AFAL-TR-72-289, Volumes I and II, Contract F33615-71-C-1918, SCI Systems, Inc., April 1973.

(4) Digital Systems: Hardware Organization and Design, F. Hill and G. Peterson, John Wiley and Sons, 1973.

(5) "Standard Multiplex Interface Definition for Advanced Aircraft Avionics", AFAL-TR-74-132, Volume I, Contract F33615-73-C-1222, SCI Systems, Inc., July 1974.

(6) "An Empirical Examination of Digital Signal Transmission in a Shielded, Twisted Cable", Mitre Working Paper Nr. WP 5601, February 13, 1974.

APPENDIX A

LOWER OPERATING FREQUENCY ON THE BUS

GENERAL

One MHz bus operation is not considered unreasonable where mandated by the true signal flow requirements of the aircraft in which the system is installed. For one thing, it appears that that frequency is within the bandwidth capability of a twisted shielded wire pair of lengths which would ordinarily be encountered in physical installations. It also seems that acceptable engineering compromises have been worked out among power levels, isolation and termination resistor values, bus to terminal couplers and maximum bit error rates such that satisfactory performance can be obtained.

ITEMS TO CONSIDER

As with any technical compromise, however, certain costs are involved. Rather than there being a clearly defined upper frequency at which the bus conveniently can be operated, it would appear that problems such as line reflections, jitter, interpulse interference and waveform distortion simply increase fairly rapidly with frequency. Accordingly it seems wise to maintain the bus frequency as low as possible consistent with the bit transfer load requirement plus a requirement to standardize the rate. On this latter point is is suggested that three standard rates be set up; 1 MHz for large and high performance aircraft, an intermediate rate (say 500 or even 250 KHz) for medium performance, medium sized aircraft, and a low rate (say 50 or 100 KHz) for small aircraft.

Take the Command/Response method as an example. Supposedly, the Central Bus Controller CC executes computer-like instructions at a rate several times the bus rate. This might be at 5 MHz and CC divide by 5 to set the 1 MHz bus rate. Conceivably controller and terminal circuits which are presently postulated to work at 1 MHz could be designed so that they will work anywhere between 50 KHz and 1 MHz. Then the required change among aircraft classes would be in the number of frequency dividers.

BUS FREQUENCY FACTORS

A double barrelled deleterious effect is encountered with increasing frequency, with regard to line reflections, wave pattern distortion and the like.

(1) The intensity of the phenomena increases. This is due primarily to the difficulty of accomplishing anything like correct impedance matching as the signals become wideband. (See the paragraph titled CABLE TERMINATION, below.) A second order effect is that a bandwidth limitation is just starting to show up at 1 MHz for large installations. (6), pages 24 and 25.

(2) The practical difficulty of coping with the phenomena increases. This is because the bit pulse width varies inversely with the frequency. The narrower the bit, the more precise in its action the device or circuit which "measures" the pulse in order to identify it must be. These are the problems of detection, bit sync, "slicing level",

(6) "An Empirical Examination of Digital Signal Transmission in a Shielded, Twisted Cable", Mitre Working Paper Nr. WP 5601, February 13, 1974.

and others.

CABLE TERMINATION

Quoting from (3), page 100, "Test results indicate that the characteristic impedance Z_o for most cables is equivalent to a resistor and capacitor in series, such that for optimum matching the complex conjugate, a resistor and inductor in series should be used. If a narrow band signal is used, optimum matching could be obtained, but for a wide band signal the matching network would be very complex."

It appears that the shunt coupling technique using isolation resistors called for in the MIL-STD is a very inefficient coupling technique and subject to severe interpulse interference and bandwidth limiting. Mr. Larry Gutman, AFAL/AAI, in a memo for record dated 19 June 74, has suggested an inductive toroid transmission line matching circuit which looks very interesting.

APPENDIX B

SIGNAL FLOW DATA

SCI's RAW DATA

SCI's signal list for the night AX was in the form of 35 computer printout pages in Appendix D of (3). A sample page is reproduced as Table B-1 to show the general format and the degree of detail involved. SCI reduced that data to a second computer printout of 24 pages, titled "Night AX TDM Signaling Breakdown". See Appendix P, Volume II, of (3). That breakdown consisted of signal counts, by terminal and by analog (g), discrete (d) or digital/numeric (w) type. The signals were further broken down by sampling rate (S/S) and also by bits per sample (word) for the analog and digital numeric types. Sample sheets for one of the terminals, Terminal T-4, are reproduced as Table B-2.

ADDITIONAL PROCESSING

Additional processing steps by the writer were to

Cross out the intra terminal signals because of SCI's conclusion, page 52 of (3), that "the amount of cabling required to directly connect LRU's within a terminal area is less than if they are all brought to the terminal unit and connected through it."

Scale down our example to include only sampling rates of 1, 5, 10, 20 and 40 S/S. This required reclassifying one digital numeric signal from 25 S/S to 40 S/S permitting elimination of the 25 S/S category entirely.

List the remaining signals, in a table not shown, by

NIGHT AX AVIONICS
SCI-E076

TARGET ACQUISITION AND WEAPON DELIVERY

DESIG-NATION	SIGNAL NAME	WR	TO	CL	CR	LT	DS	CB	LA	APP	DIST	RCN	CLAS	MIN BITS /WD	MIN SAM /SEC	DESTINATION(S) 1	2	3	4	REMARKS	CARD NP
TD4B1 G	DIVE CUE				X	X	X	X		A	40	1	ALC	01	5	TD4A					1 A
TD4B1 H	SCAN NAR/WIDE				X	X	X	X		A	40	1	ALD	01	5	TD4A					1 A
TD4B1 J	Z DEPRESSION				X	X	X	X		A	40	1	ALA	10	20	TD4A					1 A
TD4B1 K	X DEPRESSION				X	X	X	X		A	40	1	ALA	10	20	TD4A					1 A
TD4B1 L	CODE				X	X	X	X		A	40	1	ALW	13	20	TD4A					1 A
TD4B1 M	CODE RET				X	X	X	X		A	40	1				TD4A					1 A
TD4B1 R	GND				X	X	X	X			02	1	PWR			PR5					1 A
TD4B1 S	PIP/PRF SEL				X	X	X	X		A	40	1	ALD	01	5	TD4A					1 A
TD4C1 A	CUE DIR CCS X				X	X	X	X		A	23	1	ALA	10	20	TD4A					1 A
TD4C1 B	CUE DIR CCS Y				X	X	X	X		A	23	1	ALA	10	20	TD4A					1 A
TD4C1 C	CUE DIR CCS Z				X	X	X	X		A	23	1	ALA	10	20	TD4A					1 A
TD4C1 G	7VRMS 400HZ REF				X	X	X	X			23	1	PWR			TD4A					1 A
TD4C1 K	TEMP WARN OUT				X	X	X	X		A	20	1	ALD	01	1	MS3					1 A
TD4C1 W	TRACK LAMP				X	X	X	X		A	18	1	ALD	01	5	TD7B	MS8				1 A
TD4C1 X	TGT AZ X				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C1 Y	TGT AZ Y				X	X	X	X		A	12	1	ALA	10	1	TD7B					1 A
TD4C1 Z	TGT AZ Z				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C1SA	TGT EL X				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C1SB	TGT EL Y				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C1SC	TGT EL Z				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C2 A	ACQ CURSOR AZ+				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C2 B	ACQ CURSOR AZ-				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C2 C	ACQ CURSOR AZC				X	X	X	X		A	12	1				TD7B					1 A
TD4C2 D	ACQ CURSOR EL+				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C2 E	ACQ CURSOR EL-				X	X	X	X		A	12	1	ALA	10	20	TD7B					1 A
TD4C2 F	ACQ CURSOR ELC				X	X	X	X		A	12	1				TD7B					1 A
TD4C2 G	MODE CUE				X	X	X	X		A	12	1	ALD	01	5	TD7B					1 A
TD4C2 J	115V PWR RET				X	X	X	X			02	1	PWR			PR5					1 A
TD4C2 L	28VDC PWR RET				X	X	X	X			02	1	PWR			PR5					1 A
TD6A1 B	GND	X	X	X	X	X	X	X	X		02	1	PWR			PR5					1 A
TD6A2	RF IN/OUT	X	X	X	X	X	X	X	X	A	02	1	AHA			TD6C				COAX	1 A
TD6A3 A	+20VDC	X	X	X	X	X	X	X	X	A	84	1	PWR			TD6B					1 A
TD6A3 C	BLANKING OUTPUT	X	X	X	X	X	X	X	X		67	1	AAC			MS1				CRITICAL DELAY	1 A
TD6A3 E	-10VDC	X	X	X	X	X	X	X	X		84	1	PWR			TD6B					1 A
TD6A3 F	GND	X	X	X	X	X	X	X	X		02	1	PWR			PR5					1 A
TD6B1 1	DECODE CONTROL	X	X	X	X	X	X	X	X	A	84	1	ALA	08	5	TD6A				MULT LEVEL DC	1 A
TD6B1 2	ENCODE CONTROL	X	X	X	X	X	X	X	X	A	84	1	ALA	08	5	TD6A				MULT LEVEL DC	1 A
TD6B1 5	5V RETURN	X	X	X	X	X	X	X	X		02	1	PWR			PR5					1 A
TD6B1 7	28VDC OUT	X	X	X	X	X	X	X	X		84	1	PWR			TD6A					1 A
TD6B1 8	GND	X	X	X	X	X	X	X	X		02	1	PWR			PR5					1 A
TD6B111	STANDBY	X	X	X	X	X	X	X	X	A	84	1	ALD	01	5	TD6A					1 A
TD6C1	RF IN/OUT	X	X	X	X	X	X	X	X		02	1	AHA			TD6A				COAX	1 A
TD7A1 1	HUD OFF/FAIL	X	X	X	X	X	X	X	X	A	10	1	ALD	01	1	MS3					1 A
TD7A1 2	HUD O/F RET	X	X	X	X	X	X	X	X	A	10	1				MS3					1 A

LEGEND WR WARMUP CL CLIMB LT LOITER CB COMBAT
TO TAKEOFF CR CRUISE DS DESCENT LA LANDING

TABLE B-1. SCI's Gross Data Flow Model, Sample Page

BEST AVAILABLE COPY

SOURCE TERMINAL 4 ANALOG LISTING

SINK TERMINAL 1

MIN SAM/SEC	5	10	20	250	300	500
MIN BITS/WD						
4	0	0	0	0	0	0
5	0	0	1	0	0	0
6	0	0	5	0	0	0
7	0	0	0	0	0	0
8	0	0	0	0	0	0
10	0	0	0	0	0	0

SINK TERMINAL 2

MIN SAM/SEC	5	10	20	250	300	500
MIN BITS/WD						
4	0	0	0	0	0	0
5	0	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
8	0	0	0	0	0	0
10	0	0	0	0	0	0

SINK TERMINAL 3

MIN SAM/SEC	5	10	20	250	300	500
MIN BITS/WD						
4	0	0	0	0	0	0
5	0	0	0	0	0	0
6	0	0	3	0	0	0
7	0	0	10	0	0	0
8	0	0	0	0	0	0
10	0	2	9	0	0	0

SOURCE TERMINAL 4

MIN SAM/SEC	5	10	20	250	300	500
MIN BITS/WD						
4	0	0	0	0	0	0
5	0	0	1	0	0	0
6	0	0	8	0	1	0
7	0	0	10	0	0	0
8	0	0	0	0	0	0
10	0	2	12	0	0	0

SINK TERMINAL 5

MIN SAM/SEC	5	10	20	250	300	500
MIN BITS/WD						
4	0	0	0	0	0	0
5	0	0	0	0	0	0
6	0	0	0	0	1	0
7	0	0	0	0	0	0
8	0	0	0	0	0	0
10	0	0	3	0	0	0

SINK TERMINAL 6

MIN SAM/SEC	5	10	20	250	300	500
MIN BITS/WD						
4	0	0	0	0	0	0
5	0	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
8	0	0	0	0	0	0
10	0	0	0	0	0	0

TABLE B-2. SCI's AX Signal Breakdown, Four Sample Pages

SOURCE TERMINAL 4 DISCRETE LISTING

SINK TERMINAL 1

MIN SAM/SEC	1	5	10	20	30	100	200	2K
	5	9	2	23	0	0	0	0

SINK TERMINAL 2

MIN SAM/SEC	1	5	10	20	30	100	200	2K
	14	39	4	16	0	0	0	0

SINK TERMINAL 3

MIN SAM/SEC	1	5	10	20	30	100	200	2K
	0	9	1	0	0	0	0	0

SOURCE TERMINAL 4

MIN SAM/SEC	1	5	10	20	30	100	200	2K
	19	59	8	56	0	1	2	0

SINK TERMINAL 5

MIN SAM/SEC	1	5	10	20	30	100	200	2K
	0	0	0	1	0	0	2	0

SINK TERMINAL 6

MIN SAM/SEC	1	5	10	20	30	100	200	2K
	0	2	1	16	0	1	0	0

TABLE B-2 - Page 2

DIGITAL/NUMERIC LISTING

SINK TERMINAL 1

MIN SAM/SEC	5	10	20	25	40	350
MIN BITS/WD						
2	0	0	0	0	0	0
3	0	0	0	0	0	0
4	0	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
10	0	0	0	0	0	0
13	0	0	0	0	0	0
16	0	1	0	0	0	0
32	0	0	0	0	0	0

SINK TERMINAL 2

MIN SAM/SEC	5	10	20	25	40	350
MIN BITS/WD						
2	0	0	0	0	0	0
3	0	0	0	0	0	0
4	0	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
10	0	0	0	0	0	0
13	0	0	0	0	0	0
16	0	0	0	0	0	0
32	0	0	0	0	0	0

SINK TERMINAL 3

MIN SAM/SEC	5	10	20	25	40	350
MIN BITS/WD						
2	0	0	0	0	0	0
3	0	0	0	0	0	0
4	0	0	0	0	0	0
6	0	0	0	0	2	0
7	0	0	0	0	0	0
10	0	0	0	0	0	0
13	0	0	0	0	0	0
16	0	1	0	0	0	0
32	0	0	0	0	0	0

SOURCE TERMINAL 4

MIN SAM/SEC	5	10	20	25	40	350
MIN BITS/WD						
2	0	0	0	0	0	0
3	0	0	0	0	0	0
4	0	0	0	0	0	0
6	0	0	0	0	2	0
7	0	0	0	0	0	0
10	0	0	0	0	0	0
13	0	0	0	0	0	0
16	0	2	0	0	0	0
32	0	0	0	0	0	0

TABLE B-2 - Page 3

DIGITAL/NUMERIC (Continued)

SINK TERMINAL 5

MIN SAM/SEC	5	10	20	25	40	350
MIN BITS/WD						
2	0	0	0	0	0	0
3	0	0	0	0	0	0
4	0	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
10	0	0	0	0	0	0
13	0	0	0	0	0	0
16	0	0	0	0	0	0
32	0	0	0	0	0	0

SINK TERMINAL 6

MIN SAM/SEC	5	10	20	25	40	350
MIN BITS/WD						
2	0	0	0	0	0	0
3	0	0	0	0	0	0
4	0	0	0	0	0	0
6	0	0	0	0	0	0
7	0	0	0	0	0	0
10	0	0	0	0	0	0
13	0	0	0	0	0	0
16	0	0	0	0	0	0
32	0	0	0	0	0	0

terminal and by type (g, d or w). From that table, the subsets of signals transferred from each transmitter Tr_i to each receiver Rc_j were obtained. These values, along with the total number of signals emitted by each transmitter and the total for the system, are listed in Table B-3. The example has retained 576 signals compared with SCI's 588 for the AX, a retention of approximately 98%.

PRIMARY SIGNAL DATA

The primary data needed to structure the transmission cycles are the number of bits at each S/S for each Tr_i/Rc_j combination, for all i's and j's 1 through 6. These were obtained by multiplying each signal on SCI's printout by the number of bits per signal and adding. The results are given in Table B-4. The reader is referred to the paragraphs on Cycle Definition and Cycle Notation in the body of the report for a description of how these numbers are used to establish the sizes of the cycles.

(1) The bits at the different S/S's at each Tr_i/Rc_j combination are added, and the totals are given in Table B-3.

(2) Lastly, the total bit rate was obtained. This was gotten by multiplying the bit totals at the bottom of the columns in Table B-4 by the S/S's, and adding. The total bit rate for the example proved to be 17,803 bits per second, which is slightly less than the 17,880 Hz clock rate of the system.

ACTUAL BIT ALLOCATIONS TO THE BUS

At the bit level, which is the fine grain structure, bits are assigned slots on the bus in the order in which they appear in the

Into Terminal, from Bus, Rc_j

Out of Terminal, on to Bus, Tr_i

i \ j		1	2	3	4	5	6	TOTALS
1	Sigs		3	85	22	10	-	120
	Bits		3	162	42	49	-	256
2	Sigs			97	84	5	5	191
	Bits			200	84	5	19	308
3	Sigs	25	10		5	1	14	55
	Bits	93	26		33	10	14	176
4	Sigs	48	73	39		4	19	183
	Bits	92	73	253		31	19	468
5	Sigs	2	5	-	6		-	13
	Bits	2	5	-	33		-	40
6	Sigs	-	3	10	1	-		14
	Bits	-	3	31	1	-		35
								576 Signals
								1283 Bits

TABLE B-3. Signal and Bit Totals by Transmitter-Receiver Combinations, for the A-10 Example

Cycle End, CE	44			306			59			34			4		
S/S	40's			20's			10's			5's			1's		
ij	X,Y	Splits	Bits	X,Y	Splits	Bits	X,Y	Splits	Bits	X,Y	Splits	Bits	X,Y	Splits	Bits
43			12			178			53			10	5,1		
41						58	3,1	6 +12	18	4,1 (34		11		4 +1	5
42						16	(59 Bits)		4	Bits)	13 +26	39	5,2	3	14
45				2,1		31							5,3 ← 4		
46				(306 Bits)		16			1			2	5,4 ← 3 5,5 ← 3	1	
51						1				4,2		1			
52						2				(34		3	5,6		
54					4 +26	30				Bits)		2	(3		1
62						2	3,2						Bits)		1
63						28	(59			4,3		1			2
64						1	Bits)			(34 Bits)			5,7		
13	1,1		32			49			7		33 + 7	40		1	34
12	(44														3
14	Bits)					26				4,4		16			
15				2,2		43				(34 Bits)		6			
23				(305		60		35 +35	70		5 +8	13			57
24				Bits)		2			1	4,5	26	81			
25						1	3,3			4,6	34 +21	4			
26							(59			4,7 (33	8 +11	19			
31						40	Bits)	23 +16	39	Bits)		12			2
32									12	4,8		10			4
34						13	3,4		20	(33					
35							(58		10	Bits)					
36						14	Bits)								
Totals			44			611			235			270			123

FIGURE B-4. Bit Time Allocations on the Bus

columns of Table B-4. The number of bits which can be accommodated in the respective cycle groups are printed across the top line of the table. The manner in which these numbers were derived was described in the body of the report in the section titled TIMING ON THE BUS. The procedure is to go down the columns of Table B-4, filling each X,Y cycle as indicated in the first column of each S/S, as one goes along. The cases in which subsets of bits belonging to a particular transmitter-receiver combination and S/S have to be split in order to fill the cycle groups, are shown in the second column of each S/S. These are the sources of probable sample splits mentioned in the body of the report. The allocation for the 1's in the table was not completed because the job was tedious and the main objective was to demonstrate the procedure. The values of Table B-4 listed by transmitter terminal, and subscripted to indicate the corresponding receiving terminal, are next transferred to Table B-5, where they show up in the columns headed CM_T. There they are used as a cross check on the computed values of Begin Transmit BT, End Transmit ET and the start address SA_T in the transmitter buffer memory. As an example of the transfer of numbers from Table B-4 to Table B-5, consider the 28 bits of the 20 samples/sec that go from T-6 to T-3 ($i = 6$, $j = 3$). They are in cycle X,Y = 2,2, Table B-4. On Table B-5, they are found under CM_T under the T-6 column, in the row X,Y = 2,2 as $(28)_3$.

CALCULATION OF BT, ET AND SA_T

The values of Begin Transmit, BT, are obtained by counting the number of bits in the cycle which have preceded a given terminal's

X,Y	T-4				T-5				T-6				T-1				T-2				T-3			
	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T
1,1	1	13	1	$(12)_3$									13	45	1	$(32)_3$								
2,1	1		13	$(178)_3$	300		1	$(1)_1$																
				$(58)_1$				$(2)_2$																
				$(16)_2$		307		$(4)_4$																
				$(31)_5$																				
		300		$(16)_6$																				
3,1	1		312	$(53)_3$																				
		60		$(6)_1$																				
4,1	1		371	$(10)_3$																				
				$(11)_1$																				
		35		$(13)_2$																				
5,1	1	5	405	$(4)_1$																				
2,2					1	27	8	$(26)_4$	27		1	$(2)_2$	58		33	$(49)_3$	176		1	$(60)_3$	239		1	$(40)_1$
												$(28)_3$				$(26)_4$				$(2)_4$				$(13)_4$
										58		$(1)_4$		176		$(43)_5$		239		$(1)_5$		306		$(14)_6$
3,2	1		409	$(12)_1$									18	25	151	$(7)_3$	25	60	64	$(35)_3$				
				$(4)_2$																				
		18		$(1)_6$																				

FIGURE B-5. Transmitter Stored Values. Begin Xmt BT, End Xmt ET, and Start Addresses SA_T in Buffer Memory CM_T (Continued)

X,Y	T-4				T-5				T-6				T-1				T-2				T-3			
	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T
4,2	1		426	$(26)_2$	29		34	$(1)_1$																
		29		$(2)_6$				$(3)_2$																
						35		$(2)_4$																
5,2	1		454	$(1)_1$																				
		5		$(3)_2$																				
3,3																	1		99	$(35)_3$	37	60	68	$(23)_1$
																		37		$(1)_4$				
4,3									1	2	32	$(1)_3$	2	35	158	$(33)_3$								
5,3	1	5	458	$(4)_2$																				
3,4																					1		91	$(16)_1$
																								$(12)_2$
																								$(20)_4$
																						59		$(10)_5$
4,4													1		191	$(7)_3$	30	35	135	$(5)_3$				
																$(16)_4$								
														30		$(6)_5$								
5,4	1	4	462	$(3)_2$																				
4,5																	1		140	$(8)_3$				
																		35		$(26)_4$				

FIGURE B-5. (Continued)

X,Y	T-4				T-5				T-6				T-1				T-2				T-3			
	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T	BT	ET	SA_T	CM_T
5,5	1	4	465	$(3)_2$																				
4,6																	1	35	174	$(34)_4$				
5,6	1	2	468	$(1)_2$	2	3	40	$(1)_4$	3	4	33	$(1)_2$												
4,7																	1		208	$(21)_4$				
																				$(4)_5$				
																		34		$(8)_6$				
5,7									1	3	34	$(2)_3$	3	4	220	$(1)_3$								
4,8																	1	12	241	$(11)_6$	12		149	$(12)_1$
																						34		$(10)_2$

FIGURE B-5. (End)

transmission. These computations are made using Table B-4. Consider, for example, T-5's transmission at 20 S/S, X,Y = 2,1. The single bit $(1)_1$ is transferred after T-4 has transmitted 299 bits. $(1)_1$ is the 300th bit in the cycle, so the BT value is 300 which is entered in Table B-5.

<u>End Transmit, ET</u>. Continuing the example, the seven bits transmitted by T-5 are the last of those in cycle X,Y = 2,1. ET = 307 means that transmission was shut down right after the 306th bit was transmitted.

<u>Start Address, SA_T</u>. This computation is quite simple; merely consisting of going down the SA_T columns of Table B-5 by terminal, and writing down starting addresses in Transmitter Buffer CM_T on a cumulative basis. For example, consider X,Y = 2,2 Terminal T-5. Seven bits already have been stored in CM_T, for X,Y = 2,1. Hence the SA_T for X,Y = 2,2 is 8.

RECEIVER PARAMETERS, TABLE B-6

First, bits for a given X,Y cycle are transferred from the CM_T columns of Table B-5 to the CM_R (receiver buffer memory) columns of Table B-6, in order. Secondly, the BR values are computed by calculating, using Table B-5, the number of bits which have preceded that reception in the cycle. Going down the IA column for a terminal, Indirect Address "first" locations (see Figure 11) are numbered in sequence. Start Addresses SA_R in CM_R are likewise numbered in order exactly as was done for CM_T's SA_T's in Table B-5.

(1) Consider as an example, the 16 bits which are sent from T-4 to T-2 in cycle X,Y = 2,1. These appear in a CM_T column in Table

X,Y	T-4					T-5					T-6					T-1					T-2					T-3				
	BR	ER	IA	SA_R	CM_R	BR	ER	IA	SA_R	CM_R	BR	ER	IA	SA_R	CM_R	BR	ER	IA	SA_R	CM_R	BR	ER	IA	SA_R	CM_R	BR	ER	IA	SA_R	CM_R
1,1																										1		1	1	$(12)_4$
																											45			$(32)_1$
2,1	303	307	1	1	$(4)_5$	253	284	1	1	$(31)_4$	284	300	1	1	$(16)_4$	179	237	1	1	$(58)_4$	237	253	1	1	$(16)_4$	1	179	3	45	$(178)_4$
																300	301			$(1)_5$	301	303			$(2)_5$					
3,1																54	60	5	60	$(6)_4$						1	54	5	223	$(53)_4$
4,1																11	22	7	66	$(11)_4$	22	35	5	19	$(13)_4$	1	11	7	276	$(10)_4$
5,1																1	5	9	77	$(4)_4$										
2,2	1	27	3	5	$(26)_5$	133	176	3	32	$(43)_1$	292	306	3	17	$(14)_3$	239	279	11	81	$(40)_3$	27	29	7	32	$(2)_6$	29		9	286	$(28)_6$
	57	58			$(1)_6$	238	239			$(1)_2$																	107			$(49)_1$
	107	133			$(26)_1$																					176	236			$(60)_2$
	236	238			$(2)_2$																									
	279	292			$(13)_3$																									
3,2											17	18	5	31	$(1)_4$	1	13	13	121	$(12)_4$	13	17	9	34	$(4)_4$	18		15	423	$(7)_1$
																											60			$(35)_2$
4,2	33	35	13	73	$(2)_5$						27	29	7	32	$(2)_4$	29	30	15	133	$(1)_5$	1	27	11	38	$(26)_4$					
																					30	33			$(3)_5$					
5,2																1	2	17	134	$(1)_4$	2	5	15	67	$(3)_4$					
3,3	36	37	15	75	$(1)_2$											37	60	19	135	$(23)_3$						1	36	17	465	$(35)_2$
4,3																										1		19	500	$(1)_6$
																											35			$(33)_1$

FIGURE B-6. Receiver Stored Values: Begin Rcve BR, End Rcve ER, Indirect Address Start IA, and Start Address SA, in Memory CM_R (Continued)

X,Y	T-4 BR	T-4 ER	T-4 IA	T-4 SA_R	T-4 CM_R	T-5 BR	T-5 ER	T-5 IA	T-5 SA_R	T-5 CM_R	T-6 BR	T-6 ER	T-6 IA	T-6 SA_R	T-6 CM_R	T-1 BR	T-1 ER	T-1 IA	T-1 SA_R	T-1 CM_R	T-2 BR	T-2 ER	T-2 IA	T-2 SA_R	T-2 CM_R	T-3 BR	T-3 ER	T-3 IA	T-3 SA_R	T-3 CM_R
5,3																					1	5	17	70	$(4)_4$					
3,4	29	49	17	76	$(20)_3$	49	59	7	76	$(10)_3$						1	17	21	158	$(16)_3$	17	29	19	74	$(12)_3$					
4,4	8	24	19	96	$(16)_1$	24	30	9	86	$(6)_1$																1 30	8 35	21	534	$(7)_1$ $(5)_2$
5,4																					1	4	21	86	$(3)_4$					
4,5	9	35	21	112	$(26)_2$																					1	9	25	546	$(8)_2$
5,5																					1	4	23	89	$(3)_4$					
4,6	1	35	23	138	$(34)_2$																									
5,6	2	3	25	172	$(1)_5$																1 3	2 4	25	92	$(1)_4$ $(1)_6$					
4,7	1	22	27	173	$(21)_2$	22	26	11	92	$(4)_2$	26	34	9	34	$(8)_2$															
5,7																										1	 4	27	554	$(2)_6$ $(1)_1$
4,8											1	12	11	42	$(11)_2$	12	24	23	174	$(12)_3$	24	34	29	94	$(10)_3$					

FIGURE B-6. (End)

B-5 as $(16)_2$, and are transferred to the T-2 receive column of Table B-6 as $(16)_4$. BR is 237 because 236 bits, $(178)_4$ plus $(58)_4$, have preceded this reception epoch in the cycle. ER is 253 because reception ends on the bit after the 16 bits have been received (236 + 16 = 252). IA is 1 as is SA_R because these are the first respective entries going down the T-2 columns.

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